9.4 A Multi-Coil Scalable Energy-Shared Wireless Power Receiver Network for Distributed Time-Division-Multiplexing Somatosensory Cortex Stimulation

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Abstract

This work presents a system-level scalable wireless power receiver (RX) network for miniaturized distributed somatosensory cortex stimulation. By interconnecting the power outputs of all RX cells in the network, the stimulator in each cell can access the total received power of the whole network, with a time-division-multiplexing stimulation manner. Thus, each cell owns a multiple-input single-output wireless power RX network without additional RX coils, with improved efficiency and robustness.

Brain-computer interfaces (BCIs) hold great promise for restoring motor and sensory function in individuals with severe limb disabilities. Recent advances have enabled intuitive somatosensory feedback, such as touch, vibration, and force sensations, from contact events in brain-controlled bionic limbs, significantly improving their usability and user acceptance [1, 2]. Delivering precise tactile feedback requires distributed micro-stimulation across large cortical neuron networks [3], often demanding hundreds of independently driven stimulus channels placed across multiple neural sites. Minimizing device dimensions to reduce foreign body reactions and inflammation further complicates power delivery, making wireless power transfer (WPT) indispensable. Near-field resonant inductive powering is widely used; however, the small size of the receiver (RX) coil in typical two-coil links results in a very low power transfer efficiency [4-7], along with limited transmission distance and poor robustness to frequent micromotions of the brain. Recent efforts have improved robustness using an omnidirectional wireless power reception, but the required 3D coil geometries increase the RX volume [8]. Three-coil configurations, which add a relay coil in the implant plane, can enhance efficiency and extend range by partially compensating for misalignments [3, 9-11], and have thus become widely adopted. Yet, due to the large size mismatch between the external transmitter (TX) and miniature RX coils, gains from the relay alone remain limited and typically must be combined with additional system- and circuit-level optimizations. In this work, we present a scalable system-level wireless power RX network tailored for miniaturized distributed stimulation. By interconnecting the power outputs of all RX cells in the network, the stimulation site in each cell can access the total received power of the entire network through a time-division multiplexing (TDM) stimulation scheme. As a result, every cell effectively benefits from a multiple-input single-output wireless power RX network without requiring additional RX coils, achieving improved efficiency and enhanced robustness.

Figure 9.4.1 (top) illustrates the distributed BCI concept powered by the proposed RX network. The network is implemented on a flexible PCB substrate that interconnects scalable RX cells, enabling energy sharing and distribution across all cells while preserving their free-floating characteristics. The RX network offers three key features: (1) Interconnecting the power-stage outputs of all RX cells allows each cell to access the total received power of the entire network; (2) Even under severe coil misalignment, an individual cell can still receive energy through the network from other better-aligned cells, thereby imporving robustness; (3) Each cell can initiate leader-follower control of other cells' power stages through the control interconnect, ensuring proper regulation of output power. This work demonstrates power transfer and sharing from a single TX to a three-cell chip-based RX network, and the architecture readily scales to ab arbitrary number of cells (N) without loss of generality.

Typically, the electrical stimulus pulses occupy only a small duration of the stimulation priod, and thus this work employs TDM stimulation to maximize each RX cell's power. Figure 9.4.1 (bottom) shows a wireless micro-stimulation system block diagram incorporating the proposed network. In multi-site TDM stimulation for distributed BCIs, different cells activate by detecting unique IDs via a forward data link. During a cell's enable phase, its stimulation function activates, and the RX network delivers power to its stimulus load via the interconnect. Thus, each cell consistently achieves multi-coil powering. As illustrated in Fig. 9.4.2 (top), in most conventional wireless power systems for distributed BCIs, each RX is powered solely by a single coil, limiting the available received power. Moreover, variations in coil orientation and position readily reduce received power, resulting in inconsistent output levels. In contrast, the wireless power RX network allows each cell to harvest energy from all networked coils, ensuring that all cells maintain consistent output power ranges. These features significantly enhance the stability and reliability of the stimulation power supply.

Figure 9.4.2 (bottom) shows the system architecture and control timing of the cell chip in the proposed RX network. In this work, a resonant current-mode (RCM) WPT scheme is adopted. In RCM operation, the LC-tank circuit undergoes multiple resonance cycles to progressively accumulate energy, which is then directly transferred to the output once the inductor is fully energized. Note that RCM WTP is ideally suited for multi-coil powering, as the resonant coil in charging phase can be regarded as a current source, and connecting multiple coils in parallel will not diminishes their effectiveness [8]. Key components of the RX cell include an RCM power stage, an RCM controller, a hysteresis comparator, and a mode-selection circuit. The output voltage is regulated through a hysteresis feedback control loop, which configures the RCM power stage into 1X and 0X modes via the hysteresis comparator. In 1X mode, the RX charges the output using RCM operation, while in 0X mode, both PMOS and NMOS transistors are turned. Since the equivalent input impedance of the power stage in 0X mode is very large, the AC current I_{AC} and the AC voltage V_{AC} are nearly negligible. The operation principle is as follows: the feedback voltage V_{FB} is compared with a reference voltage to generate the mode-control signal *MD*. When the output voltage V_{OUT} exceeds the upper bound of the hysteresis window, the RX enters 0X mode, temporarily halting power delivery to the output. When V_{OUT} falls below the lower bound of the hysteresis window, the RX return to 1X mode.

In the proposed wireless power RX network, any stimulus-activated cell shares the power of all other cells in the network to. In general, as shown in Fig. 9.4.3 (top), the power delivered to the load can be only adjusted by the local hysteresis feedback loop in each cell. In this way, the complexity of the control circuits design can be simplified in the system level. However, due to the difficulty of achieving good matching among key modules such as the feedback voltage divider, bandgap reference, and hysteresis comparator across different chips, offsets occur in the hysteresis window. This reduces system stability and increases output ripple. Overall, the lack of direct output power control poses safety risks, which is unacceptable for implantable medical devices. To address this issue, a control interconnection is introduced to transfer the control signal MD form the stimulus-activated cell to others, and thus all cells can share the same hysteresis feedback loop, which can be regarded as a global leader-follower hysteresis control. Note that only one hysteresis comparator is enabled, and the power loss can be reduced. In the charging phase during each RCM cycle, an exact zero-current switching (ZCS) is typically required to prevent the revise current form output to the ground once the energy of the coil is completely released. However, as shown in Fig. 9.4.3 (bottom), the frequent micromotions of the brain induce fluctuations in the power delivered to the RX LC tank, significantly altering the duration of the charging phase, which in turn varies the timing of the zero current. Therefore, the ZCS controller should promptly track the zero-current instant to further optimize efficiency. For this purpose, a simple fast zero-current tracking technique is proposed based on the common delay-line controlled ZCS. During normal operation, a dynamic comparator DCMP controls a 32b bidirectional shift register to adjust the 32b delay line with a slow digital feedback loop, and the output of DCMP will switch between '0' and '1' periodically in the steady state. If the angel/position varies, the large changing of the zero-current timing will be sensed by the 3b monitor after three consecutive RCM cycles. The signal Q[0:2] of '000' indicates that the high-side PMOS transistor was turned off too late, while '111' indicates an early turn-off. In this case, the high-side switch is forced into diode conduction mode over one resonant cycle, and this results in an optimal duration (reflected by t_{DIO}) for the charging phase. Meanwhile, t_{DIO} is quantitated by the delay line and stored in the shift register, which can be directly used in the following RCM cycles. Thus, the fast calibration is achieved.

In this work, a 3-cell RX network powered by a 3-coil link mentioned in [9] is mainly chosen to verify the functionality and the performance. The TX is implemented with a half-bridge Class-D power amplifier supplied by a 1.8V DC source. The 34mm TX coil has an inductance of 47.4nH with a quality factor (Q) of 202, while the 24mm relay coil exhibits an inductance 42.4nH and a Q of 131. For the 2mm RX coil in each cell, the simulated inductance is 22.59nH with a Q of 18.8. To verify the effectiveness of the power and control interconnection, the stimulus load of Cell 1 (emulated by the resistor R_{L1}) is activated, and the output voltage V_{OUT} is regulated using the proposed leader-follower hysteresis control, as illustrated in Fig. 9.4.4 (top). It can be clearly observed that all RCM power stages are synchronously controlled, periodically switching between 0X and 1X modes to regulate the output voltage V_{OUT}. Additionally, the resonant and charging phases in RCM wireless power receiving cycle are also distinctly visible in Fig. 9.4.4 (bottom). The measured waveforms of the TDM procedure is shown in Fig. 9.4.5 (top), demonstrating that the network power is delivered to different loads in different phases without cross regulation. Figure 9.4.5 (bottom) presents the power performance analysis of the proposed wireless power RX network. As the number of cells in the RX network increases, both the output power and the overall power transfer efficiency (PTE) improve substantially. In particular, when

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expanding to a 3-cell network yields approximately a 3× increase in output power compared to a single cell, while the efficiency improves by nearly 2.7×. Fig. 9.4.6 summarizes and compares the proposed RX network with prior work. The chip in each cell is fabricated in a 0.18μm BCD process. Photos of the TX and RX modules, along with RX and TX chip micrographs and the implant mock-up are shown in Fig. 9.4.7.

Acknowledgement:
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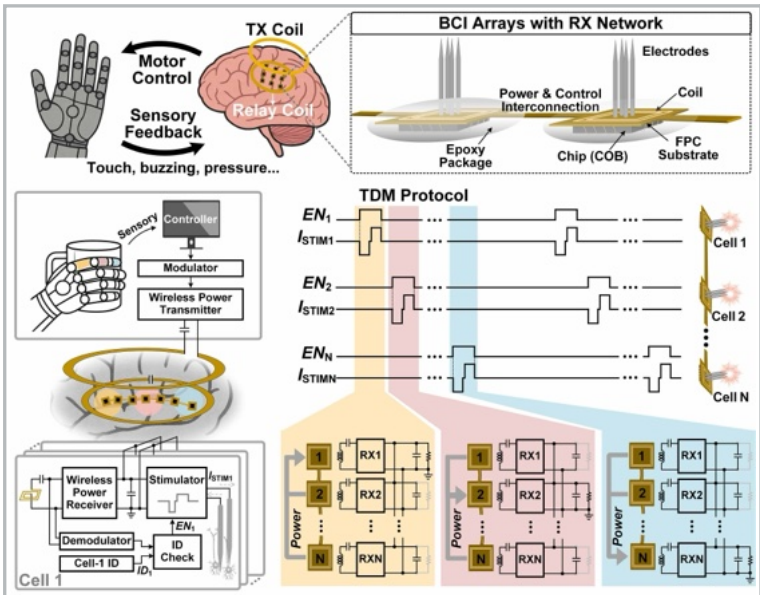

Figure 9.4.1: Concept of the proposed multi-coil scalable wireless power RX network (top). Working mechanism of the RX network based on the TDM stimulation (bottom).

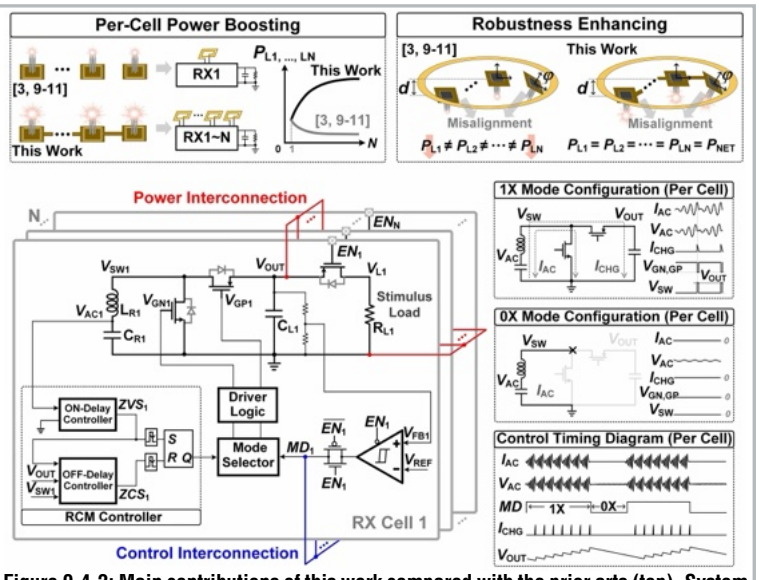

Figure 9.4.2: Main contributions of this work compared with the prior arts (top). System architecture of the RX network with the configurations and the control timing diagram of per cell (bottom).

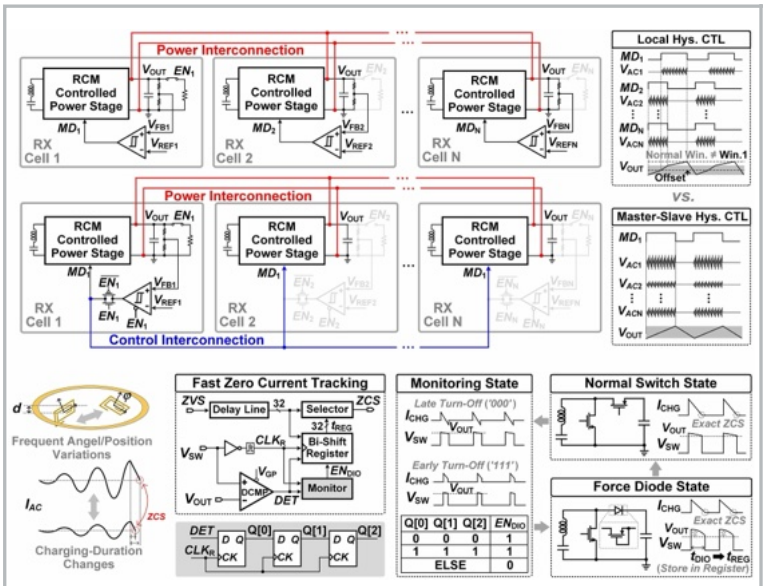

Figure 9.4.3: Detailed circuits implementation of the proposed global leader-follower hysteresis feedback control (top) and fast zero current tracking (bottom).

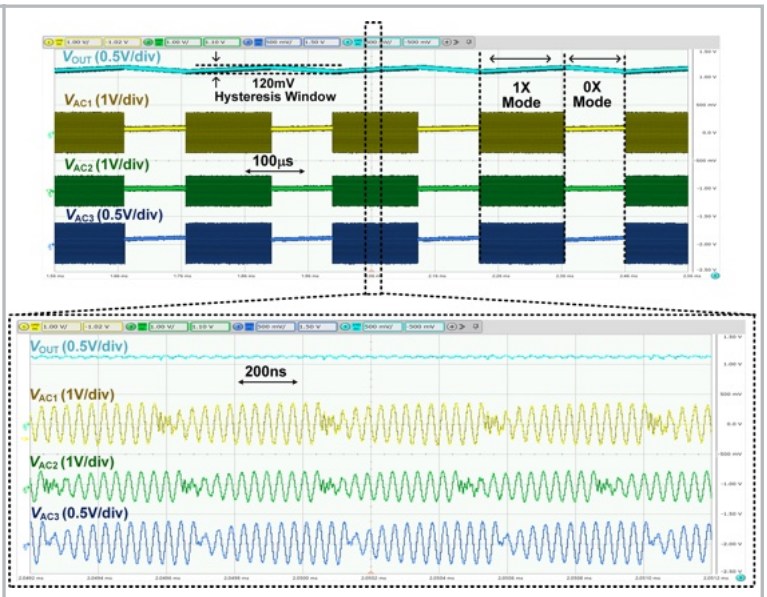

Figure 9.4.4: Measured waveforms of the power sharing, the leader-follower hysteresis control, and the detailed RCM wireless power receiving for a 3-cell RX network.

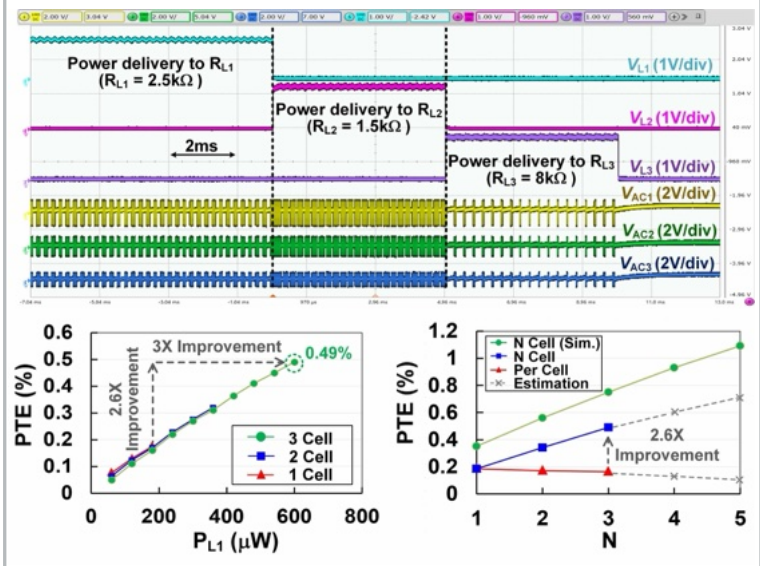

Figure 9.4.5: Measured waveforms of the TDM procedure for a 3-cell RX network (top). Measured PTE performance (bottom).

	JSSC 2013 [4]	TBCAS 2019 [5]	TBCAS 2017 [9]	ESSCIRC 2018 [10]	TBCAS 2024 [11]	This Work
IPT Link	2-Coil	2-Coil	3-Coil	3-Coil	3-Coil	3-Coil
RX Coil Size (mm²)	0.25x0.5	0.3x0.3	1x1	0.5x0.5	0.2x0.2	2x2
RX Coil Type	On-chip spiral	On-chip spiral	WWC	On-chip spiral	On-chip spiral	FPCB spiral
Frequency	1.5 GHz	1.18 GHz	60 MHz	915 MHz	433.92 MHz	27.12 MHz
TX-to-RX Coil Distance (mm)	1	6.6	16	8	14	16
Medium	Air	Beef	Air	Liquid phantom	Tissue	Air
Process (nm)	65	130	N/A	65	180	180 BCD
PTE (%)	0.021	0.0019*	2.4	0.019~0.047	0.013	0.49* (@3 Cell) 0.17* (@1 Cell)
Power Delivered to Load (µW)	10.5	55.5	1300	95~235	1970	600 (@3 Cell) 200 (@1 Cell)
Against Misalignment	No	No	Yes	Yes	Yes	Yes

*w/ rectifier.

Figure 9.4.6: Performance summary and comparison with prior arts.

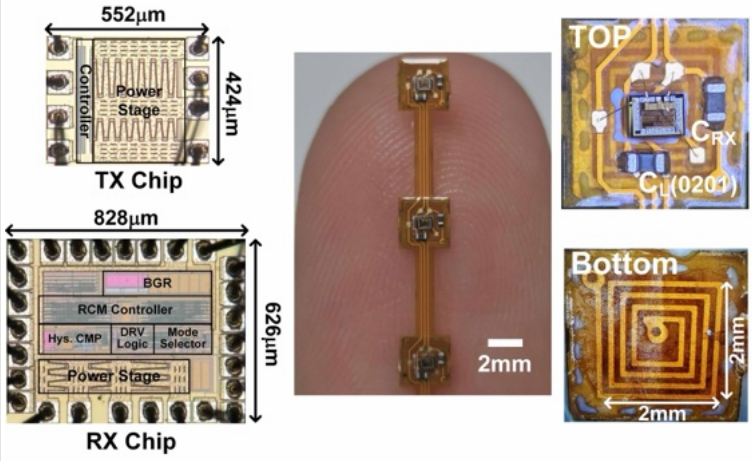

Figure 9.4.7: Chip micrographs (left) and implant mock-up (right).

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Session 10 Overview: *Digital Processing and Circuit Techniques*

DIGITAL CIRCUITS SUBCOMMITTEE

Session Chair: Visvesh S. Sathe
Georgia Institute of Technology
Atlanta, GA

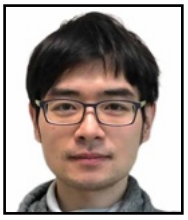
Session Co-Chair: Ping-Hsuan Hsieh
National Tsing Hua University
Hsinchu, Taiwan

Digital circuits continue to enable an increasingly broader range of applications. The first paper describes a Software-Defined Vehicle (SDV)-driven automotive 3nm SoC to achieve ASIL-D. The second paper reports energy-reliability optimizations for a mobile CPU. The next three papers explore circuit techniques for energy-efficient digital datapaths, clocking and voltage guardband reduction. In the second half of the session, advances in 3D integration are demonstrated through a 2nm-3nm hybrid-bonded die-stacked DNN processor, following by four papers that report recent advances in optimization solvers.

8:00 AM

10.1 A 3nm, 400TOPS, 1080k DMIPS SoC with Chiplet Support for ASIL D Automotive Cross-Domain Applications
Shiro Machida, Renesas Electronics, Tokyo, Japan
In Paper 10.1, Renesas presents a 312mm^2 SDV-driven automotive 3nm SoC with Freedom From Interference (FFI) functional safety techniques to achieve ASIL D. The system operates at a core voltage of 0.765V and an APU overdrive voltage of 0.865V, and comprises a 32-core APU cluster achieving 2.7GHz and 1,080k DMIPS, a 24-core NPU cluster at 1.066GHz and 400TOPS, and 51.2GB/s inter-chiplet bandwidth with UCIe.

8:25 AM



10.2 A Dynamic Performance Augmentation in a 3nm-Plus Mobile CPU
Chien-Yu Lu, MediaTek, Hsinchu, Taiwan
In Paper 10.2, MediaTek describes a dynamic performance augmentation technique for a mobile CPU, featuring boosting-duty control and an adaptive thermal cooler to boost CPU maximum performance. The 3nm-plus multicore CPU occupies 24.69mm^2 and boosts F_{max} to 4.4GHz, achieving a score of 3917 in the GeekBenchv6 single-core benchmark on a flagship smartphone, with the adaptive performance boosting circuitry consuming 0.078% of total power and 0.0122% CPU area.

8:50 AM

10.3 A 2nm Clock-Edge Architecture for Processor Clock-Power Reduction
Yimai Peng, Qualcomm, Raleigh, NC
In Paper 10.3, Qualcomm presents a 2nm NPU matrix-multiplication unit occupying 0.170mm^2 featuring dual-edge-triggered flip-flops and clock-gating circuits with an adaptive clock duty-cycle controller of 675µm^2, realizing 39-to-40% lower clock power and a total dynamic power reduction of up to 15%.

9:15 AM

10.4 A 0.008mm^2 16-to-1600MHz All-Digital Fractional Divider Using AUX-DLL for Background LMS-Based DTC Calibration
Ahmed Elkholy, Broadcom, Irvine, CA
In Paper 10.4, Broadcom presents a 7nm fractional divider with a replica-free least-mean-square-based digital-to-time converter background calibration using an auxiliary delay-locked loop. The proposed FDIV consumes 10mW at 1.6GHz, 0.9V and provides an output frequency range of 16 to 1600MHz with worst-case integrated jitter of 350fs$_{rms}$, occupying 0.008mm^2.

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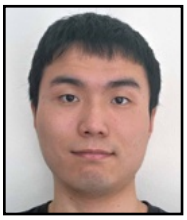
9:30 AM



10.5 Proactive Power Management-Based Supply Regulation with Online Learning for Variation-Tolerant Workload-Aware Droop Mitigation in 28nm CMOS

Xi Chen, Northwestern University, Evanston, IL

In Paper 10.5, Northwestern University presents integrated proactive power management for droop mitigation by combining a neural droop management unit, integrated high-speed power converter, and an online learning engine to combat the PDN and workload variations. The 28nm SoC, comprising a CPU operating at 1.2GHz and an accelerator operating at 600MHz under a nominal 1V supply, occupies 2.58mm^2 and achieves a peak converter efficiency of 91.7% across an output voltage range of 0.5 to 1.2V and an average of 79mV droop reduction and 48.5× throttling reduction.

10:05 AM

10.6 A Hybrid-Bonded 12.1TOPS/mm^2 56-Core DNN Processor with 2.5Tb/s/mm^2 3D Network on Chip

Phil C. Knag, Intel, Hillsboro, OR

In Paper 10.6, Intel presents a 3D stacked DNN processor leveraging hybrid bonding of Intel 18A and Intel 3 dies in a 3D network on chip design. The processor occupies 2.74mm^2 and achieves peak bandwidth of 7.0Tb/s, peak AI performance density of 12.1TOPS/mm^2 at 1.1V, 1.205GHz, and peak dynamic energy efficiency of 16.1TOPS/W at 0.5V, 280MHz.

10:30 AM

10.7 A 28nm Mode-Reconfigurable CAM-CIM Hybrid Complete 3-SAT Solver Supporting Conflict-Driven Clause Learning with 100% Solvability

Zihan Wu, Peking University, Beijing, China

In Paper 10.7, Peking University presents a 28nm complete 3-SAT solver supporting Conflict-Driven Clause Learning (CDCL) with a mode-reconfigurable CAM-CIM hybrid architecture achieving 4.0-to-8.3μs solution time for SATLIB uf/uuf50-218. The design occupies 0.65mm^2 and consumes 10.4 to 11.2mW, on average, at 0.95V, 185MHz.

10:55 AM

10.8 COBI: A Degree-of-56 Column-Bipartite Densely Connected Digital Ising Chip with 8b Spin Coefficients

Yihao Wu, University of California, Santa Barbara, CA

In Paper 10.8, the University of California, Santa Barbara, and KAIST present a 65nm digital Ising chip using a column-bipartite topology for solving combinatorial optimization problems. The chip occupies 0.483mm^2 with a spin area of 7547μm^2 and achieves sub-72ns solution time for various problems using 64 densely connected spin processing elements with 8b spin coefficients, consuming 518μW at 1.2V, 111.11MHz.

11:20 AM

10.9 SharpSAT: A Heuristic-Learning-Based SAT Accelerator Achieving 0.8μs/16.1μs Solution Time in SAT/UNSAT Cases

Aoyang Zhang, Tsinghua University, Beijing, China

In Paper 10.9, Tsinghua University presents a 28nm heuristic-learning-based SAT solver chip that uses a clause learner to efficiently explore the search space, achieving solution times of 0.8μs for SAT cases and 16.1μs for UNSAT cases having 50 variables and 218 clauses. The chip occupies 0.78mm^2 and operates at 375MHz and 0.9V, consuming 99.1mW.

11:45 AM

10.10 PCIM-SAT: A 55nm Probabilistic K-SAT Solver with p-Bit-Based Parallel-Variable Update on a Mixed-Signal Compute-in-Memory Architecture

Tinish Bhattacharya, University of California, Santa Barbara, CA

In Paper 10.10, the University of California, Santa Barbara presents a K-SAT solver with p-bit-based parallel-variable update on a mixed-signal CIM architecture. The 55nm chip achieves 5.5μs mean solution time and 265nJ mean solution energy for 50-variable and 218-clause problems operating at 1.3V, 100MHz and occupies 0.42mm^2.