9.2 A 91%-Efficiency Single-Stage Bipolar Quad-Output Regulating Rectifier with Event-Driven Output Power Enhancement via Coil-Reused DC-DC for Wireless Power Transfer

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Abstract

A bipolar quad-output regulating rectifier for wireless power transfer (WPT) is presented. Using only five power switches, it provides four independently regulated bipolar outputs. A coil-reused DC-DC mode sustains operation under heavy-load conditions beyond the RX input power limit. The rectifier achieves up to 173mW output power, 91% peak efficiency, and fast transient recovery.

Wireless power transfer (WPT) is a promising approach for non-invasive powering of biomedical implants such as neural interfaces and retinal prostheses. These advanced applications, involving large-array neural recording and multi-channel stimulation, impose stringent requirements on the WPT system. First, it must deliver multiple high-power (tens of mW) DC outputs across distinct voltage domains to supply diverse functional blocks [1-4]. Second, bipolar supplies are highly desired for neural stimulators, eliminating the need for charge pumps and full-bridge inverters [5,6]. In addition, fast load-transient recovery and event-driven heavy-load capability are critical, as implants in active mode can suddenly draw hundreds of mW for bio-modulation or wireless data transmission [4,7].

To achieve multiple regulated outputs, many designs have been proposed based on a typical full-bridge rectifier by adding additional high-side branches [1,4,8] (Fig. 9.2.1, top right). However, these lack bipolar outputs and rely on many power switches. A dual-output voltage doubler was reported in [3], providing two regulated outputs with only two switches (Fig. 9.2.1, mid left), but it remains unipolar. A dedicated bipolar-output full-bridge rectifier [9] achieves bipolar outputs, yet requires six switches, leading to low efficiency and poor hardware utilization. A bipolar current-mode rectifier using only two switches was proposed in [5] (Fig. 9.2.1, bottom left), but its bipolar outputs share a single current loop and cannot be regulated independently under variable loads. Moreover, none of the above designs can deliver higher-than-input output power to handle potential heavy loads, exposing limited operational range dependent on the RX input power levels. A DC-DC energy recycling approach [4] enhances this capability by reusing the RX coil as an inductor to transfer energy from a reservoir to a DC output, but it only supports positive regulated outputs.

To overcome these limitations, this paper proposes a single-stage bipolar quad-output regulating rectifier with coil-reusing DC-DC-enhanced heavy-load ability. The power stage uses only five switches (Fig. 9.2.1, bottom right), with the output mid-node connected to ground. M_{P1} and M_{P2} form the two positive-side branches; M_{N1} and M_{N2} constitute the two negative-side branches. Switch S_1 is activated during DC-DC operation. The rectifier delivers three stably regulated outputs, including two positive outputs, V_{OUTP1} and V_{OUTP2}, and one negative output, V_{OUTN1}. In addition, an energy reservoir (e.g., a high-density super capacitor) is employed in the negative voltage domain (V_{STO}), which can either be a regulated output or a temporary power supply. Through inverting buck–boost operation with the RX coil reused as the DC-DC inductor, V_{STO} can provisionally supply the other three outputs under event-driven heavy loads. As a result, the system maintains four bipolar regulated outputs in steady state, with three outputs sustaining heavy-load operation even when RX input power is insufficient.

The proposed rectifier operates in two modes: RX and DC-DC. In the RX mode (Fig. 9.2.2, top), S_1 is continuously ON, while M_{P1}, M_{P2}, M_{N1}, and M_{N2} function as active diodes depending on output voltage levels. When all four outputs (V_{OUTP1}, V_{OUTP2}, V_{OUTN1} and V_{STO}) are below the regulated levels, the rectifier enters the "all-ON" case with all active diodes enabled. In every two resonant periods, it cyclically operates in the sequence of $\Phi_{R1} \rightarrow \Phi_{R4} \rightarrow \Phi_{R2} \rightarrow \Phi_{R3}$, with each phase lasting for half a period, to charge V_{OUTP2}, V_{STO}, V_{OUTP1} and V_{OUTN1}, respectively, as shown in Fig. 9.2.3 (top left). If an output voltage is sufficient, its corresponding phase will be skipped. When both outputs on the same polarity are high, the rectifier allows the L_{RX}–C_{RX} tank to freely resonate in these spare phases. In addition, a 0X phase (Φ_{0X}) will be introduced to freewheel L_{RX} if all four outputs are sufficiently charged. Figure 9.2.2 (bottom left) illustrates the DC-DC mode, which relocates energy from V_{STO} to the other three outputs by reusing the existing power stage and the RX coil (L_{RX}) as a DC-DC inductor, requiring no extra components. Φ_{D1} is the L_{RX}-energizing phase, while Φ_{D2}, Φ_{D3}, and Φ_{D5} are the L_{RX}-deenergizing phases delivering power to V_{OUTP2}, V_{OUTP1}, and V_{OUTN1}, respectively. Notably, since charging V_{OUTN1} (Φ_{D5}) requires a L_{RX} current (I_{LRX}) in the other direction, an I_{LRX}-flipping phase, Φ_{D4}, is inserted, which relies on the resonant capacitor C_{RX} to fast flip I_{LRX} with low loss. Hence, the operation phase sequences to sustain the three outputs are: $\Phi_{D1} \rightarrow \Phi_{D2}$ for charging V_{OUTP2}, $\Phi_{D1} \rightarrow \Phi_{D3}$ for charging V_{OUTP1}, and $\Phi_{D1} \rightarrow \Phi_{D4} \rightarrow \Phi_{D5}$ for charging V_{OUTN1}, as shown in Fig. 9.2.3 (top right). The system workflow is presented in Fig. 9.2.2 (bottom right). Based on the hysteresis regulation of output voltages, the rectifier operates in the RX mode under normal loads; if any of V_{OUTP1}, V_{OUTP2}, and V_{OUTN1} experience undershoots due to suddenly heavier loads, the DC-DC mode will be triggered till all outputs return within their hysteresis windows.

Figure 9.2.3 (bottom) shows the system architecture in a 6.78MHz resonant WPT configuration. The five power switches, M_{P1}, M_{P2}, M_{N1}, M_{N2}, and S_1, and the 0X switch, S_{0X}, are implemented with 5V MOSFETs. M_{P1}, M_{P2}, M_{N1}, and M_{N2} employ actively biased gate and body voltages. Each of the four output voltages is monitored by a dedicated output controller. For example, V_{OUTP1} controller scales V_{OUTP1} through a multi-level resistive divider, whose three mid-nodes are compared with a reference V_{REF}, forming a hysteresis window with three levels: V_{OUTP1} is normally regulated between the upper two levels in the RX mode (indicated by EN_{RXP1}), while hitting the lowest threshold triggers the DC-DC mode (indicated by EN_{DCP1}). Notably, the V_{STO} controller uses only high and middle thresholds since V_{STO} serves as an energy reservoir that sustains the other three outputs during heavy loads while remaining regulated under normal operation.

When the rectifier operates in RX mode, 16 phase combinations arise from the four output states, each requiring a different delay-compensation strength for M_{P1}, M_{P2}, M_{N1}, and M_{N2} to achieve soft active-diode switching. Conventional fixed [10] and adaptive [11,12] delay-compensation schemes suffer from either a fixed compensation strength or slow convergence. To address this limitation, we propose a state-based delay-compensation scheme that dynamically selects the appropriate compensation strength for each active diode based on the rectifier state during the preceding half-resonant period. For example, prior to entering Φ_{R1}, the rectifier may have been operating in Φ_{R3}, Φ_{R4}, or the L_{RX}-C_{RX} free-resonance state. Accordingly, in Φ_{R1}, only the matching compensation branch in M_{P2}'s active-diode comparator is enabled with the appropriate strength. This ensures that soft switching is maintained across RX phase transitions. In DC-DC mode, constant-on-time control is applied to energize L_{RX} (Φ_{D1}), while adaptive delay compensation is used to achieve soft switching during the L_{RX}-deenergizing phases and I_{LRX}-flipping phase. Notably, all NMOS devices in the proposed system are triple-well devices with their bodies tied to V_{OUTN1}, while the chip substrate remains connected to ground, ensuring compatiblity with system-on-chip (SoC) integration.

The proposed rectifier was fabricated in a 0.18μm BCD process, occupying a silicon area of 2.84mm² (Fig. 9.2.7). In measurement, the transmitter (TX) generates a driving signal (V_S) with a peak-to-peak voltage up to 5V. The TX and RX coils have 1.137μH and 166nH inductance, and 29mm and 16mm diameters, respectively. The coils are placed coaxially with a distance of 10.2mm. Figure 9.2.4 (top) shows two measured steady-state RX waveforms. V_{OUTP1}, V_{OUTP2}, V_{OUTN1} and V_{STO} are regulated at 2.2V, 1.1V, 2.2V, and 1.8V, respectively, with ≤100mV ripples. Figure 9.2.4 (bottom) shows zoomed-in steady-state RX waveforms under different phase combinations, confirming near-optimal active-diode switching. Figure 9.2.5 (top-left) shows the load-transient waveform when R_{P1} varies between 1kΩ and 300Ω, with R_{P2}=R_{N1}=1kΩ. No undershoots or overshoots is observed at the transients, while the cross-regulation is also unnoticeable. Figure 9.2.5 (top right) shows the load-transient waveform when R_{P2} varies between 1kΩ and 300Ω, with R_{P1}=R_{N1}=1kΩ. The rectifier still shows negligible recovery time and unnoticeable cross-regulation at the transients. Figure 9.2.5 (bottom left) shows the load-transient waveform under weaker coupling conditions, and R_{P2} varies between 5kΩ and 200Ω. It is observed that V_{OUTP2} presents undershoots at the transients and under the heavier-R_{P2} condition, which trigger the DC-DC mode; the DC-DC mode further recovers V_{OUTP2} back to the preset RX hysteresis window. The zoomed-in DC-DC waveforms are shown in Fig. 9.2.5 (mid bottom) under different DC-DC phase combinations. Figure 9.2.5 (bottom right) shows the power conversion efficiency (PCE) of the proposed rectifier in the RX mode, with R_{N1}=100Ω and R_{STO}=1kΩ, under two conditions: (1) varying R_{P1} and R_{P2}=50Ω, and (2) varying R_{P2} and R_{P1}=100Ω. The peak PCE of 91% is obtained at the maximum output power of 173mW. Figure 9.2.6 shows the comparison table. The proposed rectifier realizes four regulated outputs using only five power switches, while a DC-DC mode enhances its heavy-load capability, resulting in both high PCE and high maximum output power.

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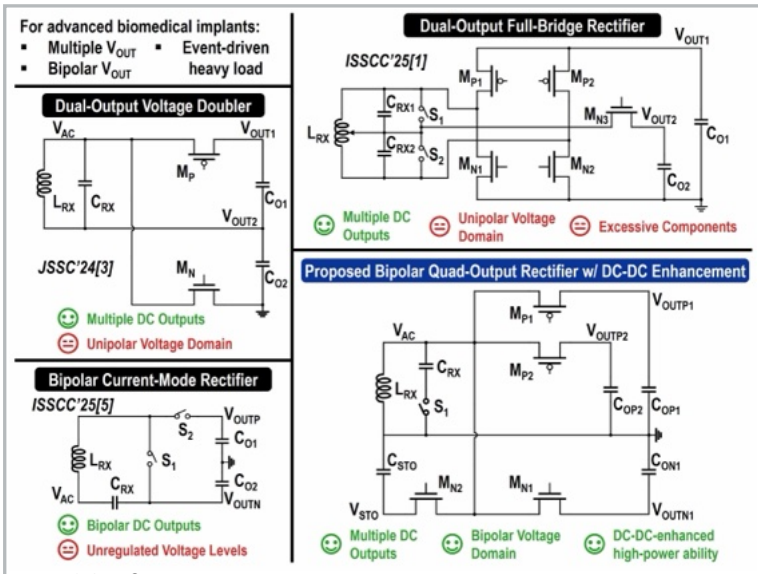

Figure 9.2.1: Conventional multi-output and bipolar-output rectifier topologies and the proposed single-stage bipolar quad-output rectifier with DC-DC-enhanced high-power ability for biomedical wireless power transfer applications.

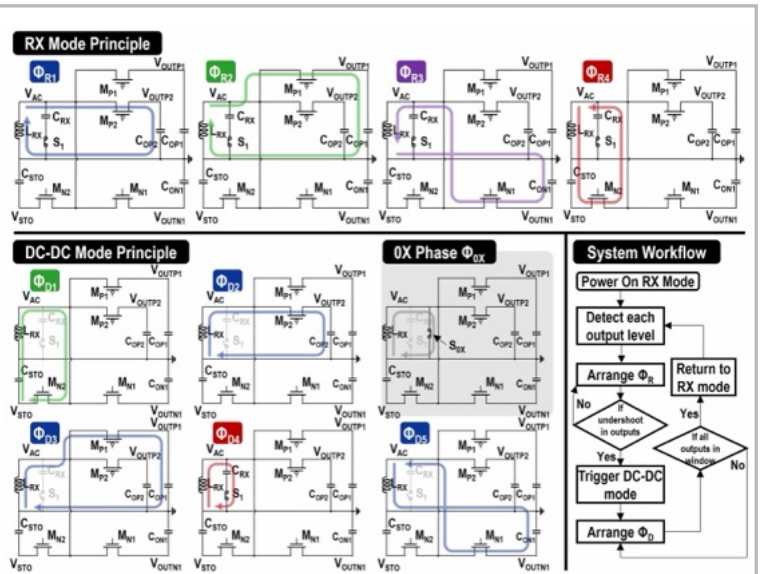

Figure 9.2.2: Operating principle of the proposed rectifier in wireless power receiver (RX) mode and DC-DC mode, and system workflow.

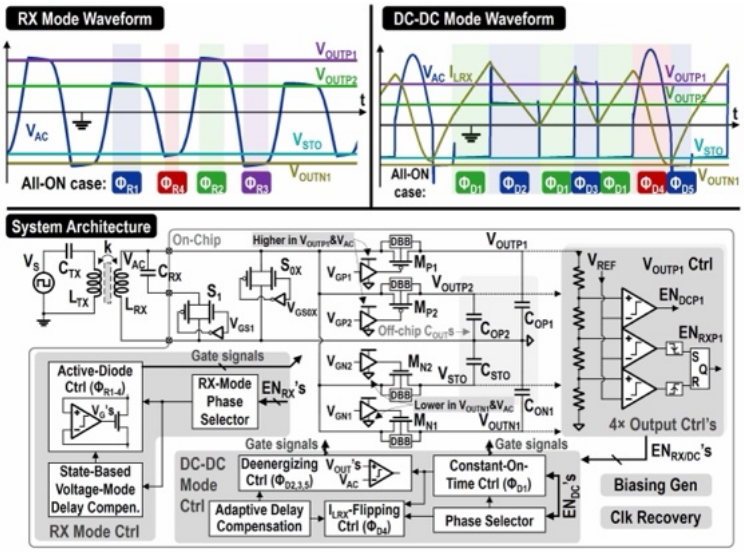

Figure 9.2.3: Operating waveform of the proposed rectifier in RX and DC-DC modes (top) and the system architecture (bottom). (DBB: dynamic body bias)

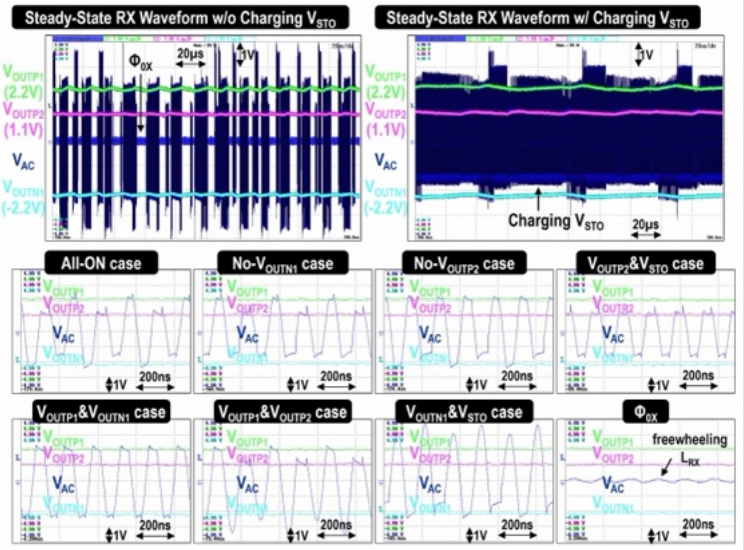

Figure 9.2.4: Measured steady-state waveform of the proposed rectifier in the RX mode (top) and zoomed-in waveforms with different phase combinations (bottom).

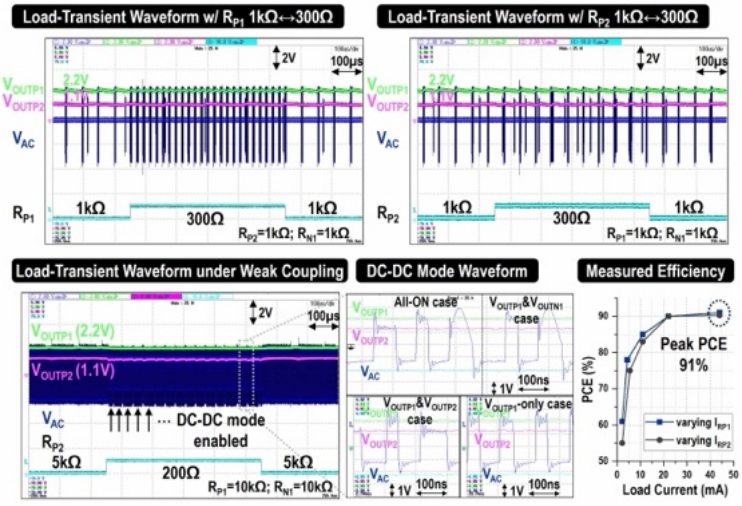

Figure 9.2.5: Measured load-transient waveforms, DC-DC mode waveform, and power conversion efficiency. (R_{P1}, R_{P2}, R_{N1} represent the load resistance at V_{OUTP1}, V_{OUTP2}, and V_{OUTN1}; I_{RP1} and I_{RP2} represent the corresponding load currents.)

	JSSC'23 [4]	JSSC'24 [9]	JSSC'24 [3]	ISSCC'25 [5]	ISSCC'25 [1]	This work
Technology	180nm CMOS	180nm BCD	180nm BCD	180nm BCD	180nm CMOS	180nm BCD
Frequency	6.78MHz	6.78MHz	6.78MHz	6.78MHz	6.78MHz	6.78MHz
LC Tank Topology	Parallel	Series	Parallel	Series	Parallel	Parallel
Chip Area	2.32mm²	8.47mm²	0.77mm²	3.24mm²	1.63mm²	2.84mm²
Number of Power Switches	6	6	2	2	5	5
Number of Outputs	2	2	2	2	2	4
Bipolar Output	No	Yes	No	Yes	No	Yes
Output Voltages	5V, 3.7V	5V, -5V	3.3V, 1.8V	1V, -1V	3.3V, 1.6V	2.2V, 1.1V, -1.8V, -2.2V
Output Ripples	35mV	45mV	100mV*	100mV*	≤75mV	≤100mV
Load-Transient Recovery Time	negligible	12µs	negligible	n/r	negligible	negligible
Cross Regulation	unnoticeable	unnoticeable	unnoticeable	n/r	unnoticeable	unnoticeable
DC-DC Enhancing Operation	Yes	No	No	No	No	Yes
Peak PCE	91.8%	86.4%	92.9%	72.5%	92.2%	91%
Maximum Output Power	300mW	5W	90.5mW	n/r	131mW	173mW

*estimated from papers. n/r: not reported.

Figure 9.2.6: Comparison table.

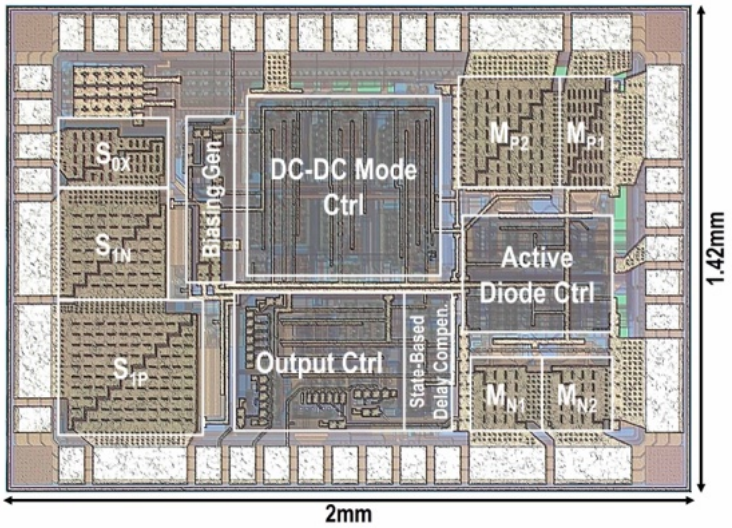

Figure 9.2.7: Chip micrograph.

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