9.1 A Single-Power-Link 13.56MHz Wireless Power and Data Transfer System with Synchronized Phase-Shifted Time-Multiplexing Dual Uplinks for Implantable Voltammetry

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Abstract

A 13.56MHz wireless power and data transfer (WPDT) system for implantable voltammetry sensor is presented. With the synchronized phase-shifted time-multiplexing technique, the system uses a single power link to support simultaneous power and two types of data transmission via dual-uplinks with neither additional coils nor efficiency degradation. The single-power-link operation is verified in silicon, measuring a 60% peak end-to-end efficiency, a fast dynamic response, and a >99.9% data linearity.

Implantable voltammetry systems play an important role in tracking biochemical activities in living organisms [1]. In implantable applications, batteries are generally not preferred due to the size, weight, risk of leakage, and the need for periodical surgical replacements. Wireless power transfer systems thus can provide a safer and long-lasting solution. To achieve higher power efficiency and reduce heat dissipation, a wireless uplink is necessary for the external transmitter (TX) to obtain feedback from the receiver (RX) to close the global loop and optimize its power transmission based on the coupling condition and loading at the implant. Wirelessly powered implantable sensors also need to retrieve digital data or analog signals with a data/signal uplink from RX to TX. Supporting two uplinks for different purposes is thus required, which poses design challenges especially with low power budget for implantable devices. Existing wireless power and data transfer (WPDT) systems typically provide only one uplink, mostly for raw data transmission only [2-4], leaving the TX operated in open loop considering maximum power transfer at worst-case scenarios, which results in energy waste and excessive heat in the coils and the implant. Some designs only provide the power uplink, with no data transmission capability [5-7]. Moreover, the uplink in previous works is often utilized with an additional coil [3] or a separated high-frequency telemetry path [4], which increases implant volume and packaging complexity or introduces cross-coupling that disturbs the power link, reducing efficiency and dynamic performance. Some WPDT systems do provide two data links, but with only one uplink while the other one is a downlink from TX to RX specifically for stimulation applications [3,4,8] or toggling between different types of the data uplink [9].

To address the needs, the paper introduces a single-power-link WPDT system with dual-uplink capability: a power uplink for global TX power regulation, and a data uplink designed for cyclic voltammetry (CV) applications, which is one of the most widely used methods for chemical sensing, with the goal of simultaneous power and dual-link data transfer without degrading power efficiency and dynamic performance.

This system is developed in conjunction with an implantable CV sensor, enabling long-term monitoring of chemical properties, for example, antibody and antigen detection, as shown in Fig. 9.1.1. The proposed system addresses the following key challenges: **1)** Efficient power transfer and fast dynamic performance. With the power uplink for closed-loop operation, the TX can adjust its power immediately based on the RX needs to avoid overpowering and heating up the coils or the implant. **2)** Dual uplinks for sensor and voltage regulation data transmission. To reduce power overhead, instead of quantizing the sensor analog information in RX and transmitting digital data, a time-based mechanism is proposed. To transmit both types of data, a synchronized phase-shifted time-multiplexing technique is proposed to process and combine the data at RX, transmit through load-shift-keying (LSK) modulation. Then, the data will be sensed, differentiated and recovered at TX. **3)** Addressing potential data conflicts and errors. This includes start-up alignment for initial phase shifting and clock correction and realignment. To address these challenges, we designed both RX and TX chips with dedicated circuits for rectification, sensing, synchronization, and data modulation, as detailed in the following sections.

RX chip Design (Fig. 9.1.2): For power conversion, an active rectifier is designed with delay compensation [8] for efficiency enhancement. A comparator is used to generate the voltage regulation request (D_{PWR_PRE}) indicating an "overpower" status when V_{FB} (representing V_0 through a fixed resistor ratio) exceeds V_{REF} for TX to reduce its transmitted power when triggered, and a current sink is used as a shunt regulator for local voltage regulation in RX. For CV sensing, the RX chip is equipped with three on-chip electrodes: the working, reference, and counter electrode (WE, RE, and CE, respectively). By applying a scanning voltage to WE with a fixed reference to RE, the current through CE contains chemical information. This current is then sensed and converted into time-based pulses (current to frequency, I2f), whose frequency is further divided by 4 before being output as the sensor data (D_{SEN_PRE}). The clock in RX (CLK_{RX}) is important as it needs to be synchronized with the TX for data recognition, so it is extracted from the AC power inputs V_{AC}s and down scaled by a 1/64 divider as CLK_{RX}. Both D_{PWR_PRE} and D_{SEN_PRE} (with the "_PRE" denoting pre-synchronization) are then synchronized to the rising and falling edge of CLK_{RX}, converted into LSK signals as D_{PWRRX} and D_{SENRX}, respectively, and transmitted by pulsing on the LSK switch briefly. The carrier V_{AC}s will be interrupted during LSK signal transmission, but because its duration and timing are initiated by and known to RX, the counters will be corrected by adding predicted counts so that the CLK_{RX} remains unaffected.

TX Chip Design (Fig. 9.1.3): For DC-AC power conversion, a Class-D power stage is designed to operate in either High-Power (HP) full-bridge mode or Low-Power (LP) half-bridge mode to drive the LC tank, controlled by D_{PMODE}. This D_{PMODE} originates from the RX, indicating RX being "overpowered". The RX generates D_{PWR_PRE}, synchronizes it as D_{PWRRX}, transmits it via LSK, and the TX recovers it as D_{PWRTX}, which directly triggers D_{PMODE}. Whenever a D_{PMODE} request is detected, the TX will switch into the LP mode for a fixed duration, which reduces a predictable amount of transmitted energy for each triggering and achieves reliable power regulation with minimized complexity. Please note that the power stage switches at 13.56 MHz, which is from an always active CLK, so not to be confused with CLK_{TX} introduced later for data identification. For data extraction, as shown in Fig. 9.1.3, the currents through the power stage will be sensed by an integrated current sensor, and the impedance change due to RX LSK signals will be recognized. To improve the detectability, a modulation depth (MD) enhancement module is designed, extracting and amplifying the voltage difference due to impedance shifts. The MD enhancement circuit captures the raw current signal V_{SENSE} and compares it with a slowly varying baseline voltage V_{CAP} that is updated through a capacitor acting as a low-pass filter. Because the intensity of HP and LP modes is different, two current sensors and MD enhancement modules are designed. The data identification will be discussed in the following section.

System Design (Fig. 9.1.4): During start up, the RX controller will bypass any LSK requests until V_{FB} crosses V_{REF} for the first time. Then the first LSK signal will be generated and transmitted, ensuring the first data is always D_{PWR}, which is used as a reference for both synchronization and data identification at TX. Enforcing D_{PWR} as the first transmitted LSK symbol also guarantees that subsequent D_{SEN} are generated only after the supply voltage for CV sensor (V_0) has reached its desired level to ensure normal sensor operation. The CLK_{RX} and CLK_{TX} have a matching frequency (1/64 of 13.56 MHz divided from CLK) but a phase shift of 90°, which not only provides the maximum detection margin but also prevents data from overlapping at the edges, thereby minimizing data ambiguity. At start up, both CLK_{RX} and CLK_{TX} stay high without switching. When the 1st D_{PWRRX} is generated at RX and received at TX as D_{PWRTX}, both CLK_{RX} and CLK_{TX} switch to low after ½ and ¼ of a cycle (creating a 180° and 90° delay), respectively, and start switching afterwards. This initiates a 90° phase shift, and D_{PWRTX} and D_{SENTX} align at the center of the high and low levels of CLK_{TX}, respectively. The phase shift between RX generating and TX receiving an LSK signal is negligible due to the 64x faster carrier frequency.

To maximize detectability and avoid error accumulation, both CLK_{RX} and CLK_{TX} will realign to 90° phase shift whenever an LSK signal is generated by RX and received by TX. This ensures that even interruptions occur, the system can automatically restore synchronization with a tolerance of up to half the detection window. To address potential data conflicts, at RX, D_{PWRRX} and D_{SENRX} are aligned to the rising and falling of CLK_{RX}, respectively, within a window of 4 carrier clocks. If a data misses the window, it is held and aligned to the next available edge. This ensures zero conflicts, and the size of the detection window is determined based on the settling time of TX LSK signal reception. However, time errors of at most a CLK_{RX} cycle may be introduced during this process. To minimize the impact of this error and ensure >99.9% linearity and <0.2% current sensing accuracy, a 2-ms averaging window is applied at readout. The averaging window could be set longer if better accuracy is needed, and will not affect the operation in our application as a CV scanning can take seconds to complete.

Both chips are fabricated in 0.18μm standard CMOS. Fig. 9.1.5 measures load transient responses and system behaviors during simultaneous power and dual-uplink data transmission, verifying the single-power-link dual-uplink WPDT operation. Measured output linearity is shown in Fig. 9.1.6, which is greater than 99.9%. Figure 9.1.6 also includes measured RX time to TX output codes. As for the current sensing accuracy, fractional Allan deviation calculated with measured TX data under different RX input frequencies (as sensor signals after I2f conversion) shows a consistent trend (white frequency noise), with the target specification of 0.2% successfully achieved at a 2-ms averaging time. As also shown in Fig. 9.1.6, up to 20.76% end-to-end (E2E) efficiency enhancement is observed by enabling the closed-loop global power control, and the impact of sensor data on power efficiency is negligible. Figure 9.1.7 shows a micrograph of both TX and RX chips along with a comparison against state-of-the-art WPDT systems. To the best of our knowledge, the

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proposed system is the only one that can transmit power with both user data/signal and global closed-loop control (dual uplink) simultaneously via a single power link, while maintaining a decent E2E efficiency.

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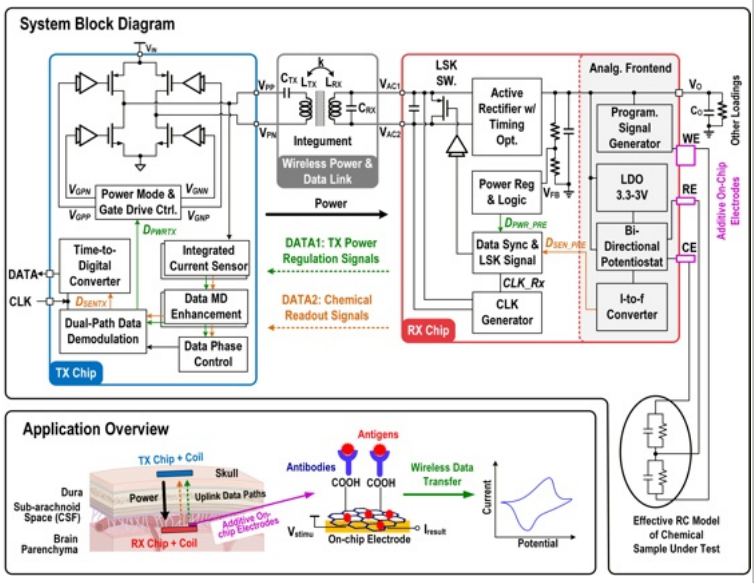


Figure 9.1.1: Proposed single-link wireless power and data transfer (WPDT) system with dual data uplinks and an application example.

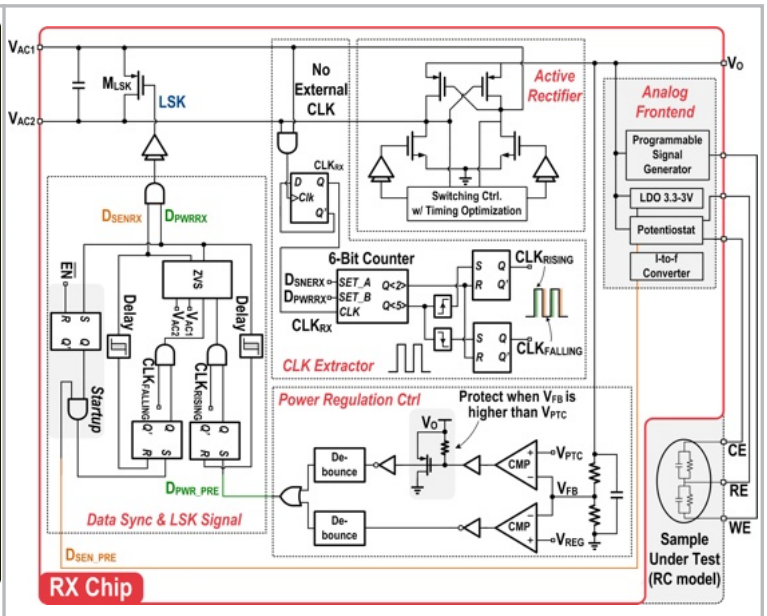


Figure 9.1.2: Detailed circuitry design of the RX chip.

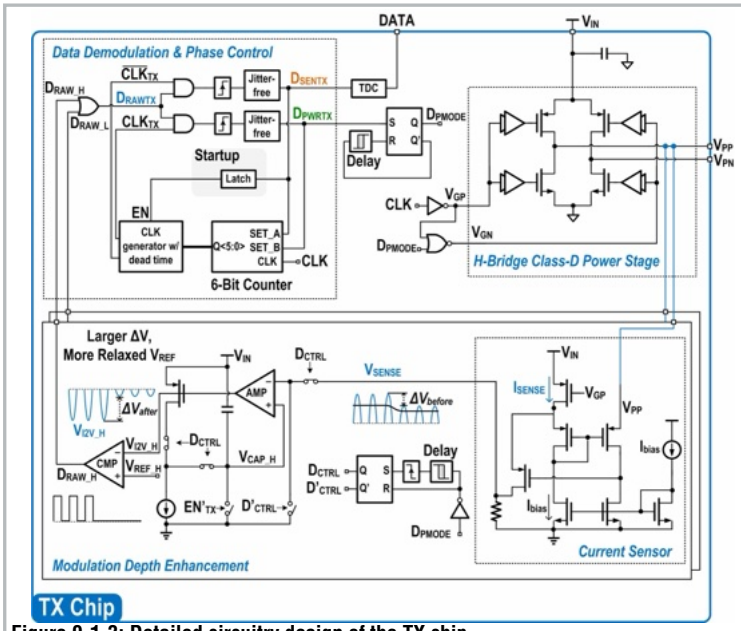


Figure 9.1.3: Detailed circuitry design of the TX chip.

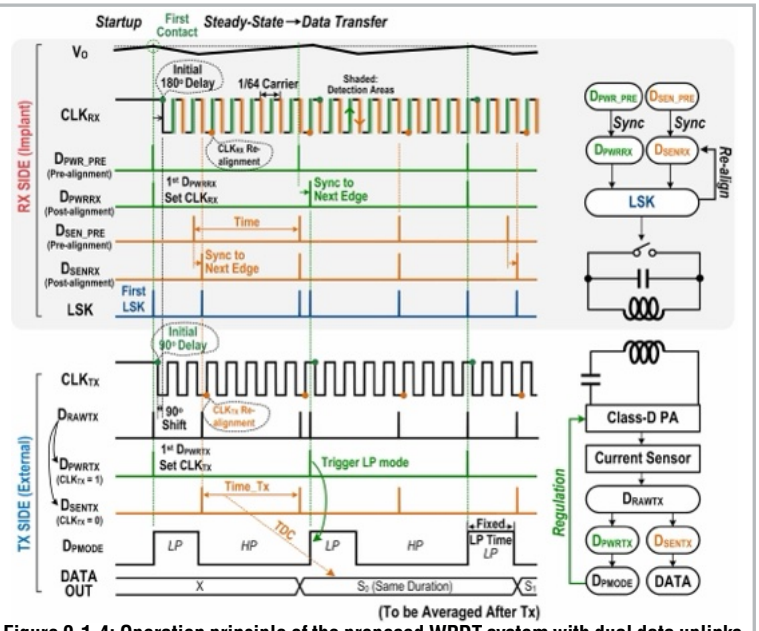


Figure 9.1.4: Operation principle of the proposed WPDT system with dual data uplinks.

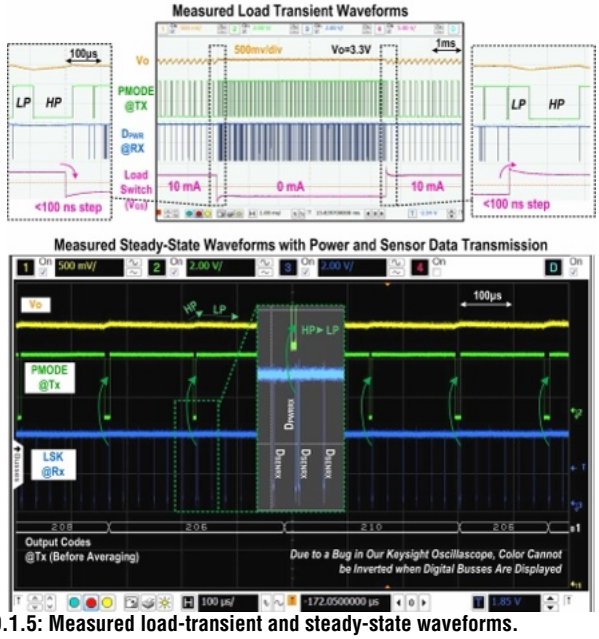


Figure 9.1.5: Measured load-transient and steady-state waveforms.

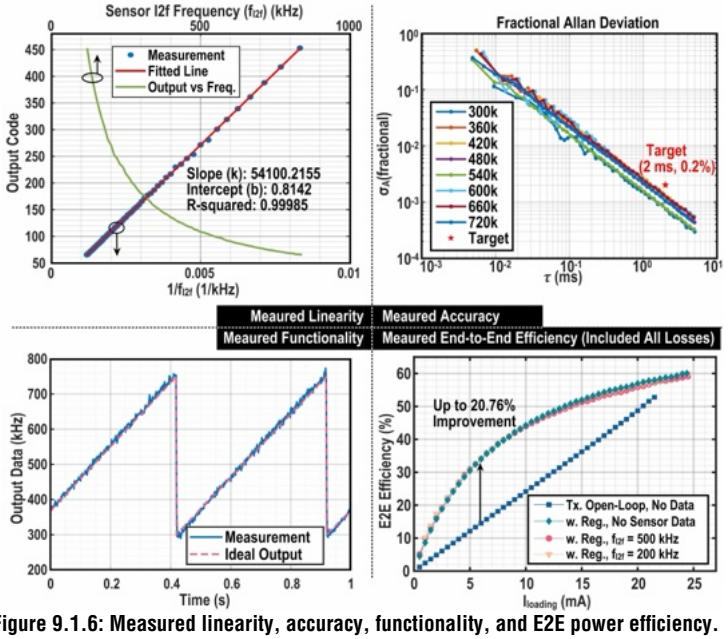
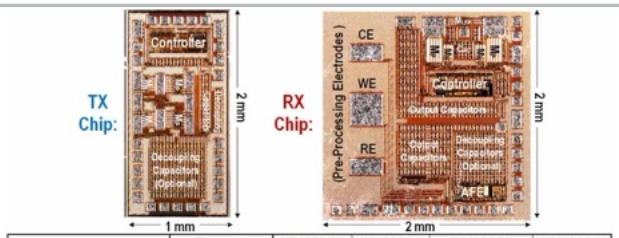


Figure 9.1.6: Measured linearity, accuracy, functionality, and E2E power efficiency.



	This work	[2] JSSC 23'	[8] JSSC 21'	[9] JSSC 24'	[10] ISSCC 21'
Technology (nm)	180 CMOS	180 CMOS	180 CMOS	65 CMOS	180 BCD
On-Silicon System Level	TX & RX	RX	RX	TX & RX	TX & RX
Frequency (MHz)	13.56	13.56	13.56	13.56	6.5/7.5
Data Modulation	LSK	OOK & LSK	ASK & LSK	LSK	FSK
Number of Data Links	2 Uplinks	1 Downlink and 1 Uplink	1 Downlink or 1 Uplink	1 Uplink	1 Downlink
TX/RX Coil diameter (mm)	24.3/18.5	30/10	N.A.	35/30	N.A.
Off-chip Sensing Component	Not required	Discrete TX	Discrete TX	55mm Dia. Sen. Coil	Not required
Data Types	Power *AND* User	User	User	Power *OR* User	User
Data Range* (kHz)	110~840[@]	N.A.			
Data Linearity*	>99.9%				
Data Format*	Time-Based Analog	Digital	Digital	Digital	Digital
Input Voltage @TX (V)	3.3	2.45	[0.5, 3]	1.2	N.A.
Output Voltage @RX (V)	3.3	2	[–3, 3]	1.2 & 2.5	N.A.
TX Closed-Loop Ctrl	Non-Linear	Open Loop	Open Loop	Linear	Open Loop
Peak E2E efficiency	60.05%	N.A.	N.A.	62.70%	56.70%
Max. Load power (mW)	79.5	2	9	20	115
ΔVo in Load Transient	Unnoticeable[#]	N.A.	N.A.	80mV/100mV[$]	N.A.
Recovery Time	Instant	N.A.	N.A.	<100µs	N.A.

*: Application specific. #: Dominated by steady-state ripples, can be further reduced by using a larger filtering capacitor.
@: Data before frequency divider to mimic the output of the sensor. $: Estimated from the measurement waveforms.

Figure 9.1.7: Chip micrographs and comparison with state-of-the-art WPDT systems.

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