8.8 A 0.292pJ/b 56Gb/s/wire Capacitively Driven Simultaneous Bidirectional Transceiver with PVT/Mismatch Tracking for XSR and D2D Interfaces in 28nm CMOS

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Abstract

A low-power (0.292pJ/b), high-bandwidth (56Gb/s/wire) single-ended capacitively driven simultaneous bi-directional (CD-SBD) TRX with PVT tolerance is proposed. Capacitive driving reduces power and self-interference in SBD. AC/DC replica and PVT/mismatch tracking provides PVT robustness without extra hardware. Per-lane CDR and a quadrature generator with QEC/DCC, secure clock margin. The TRX sustains <1e-12 BER across -6.5 to -11.5dB loss, 0.93-1.2V supply, and 0-80°C temperature variation.

Low power consumption and high bandwidth are two major priorities in XSR and die-to-die (D2D) interfaces. Figure 8.8.1(top) shows 3 signaling candidates to achieve 2× bandwidth at the same channel density as in XSR. Capacitively driven PAM-4 (CD-PAM-4) is power-efficient and provides inherent equalization (EQ) as it uses capacitive driving [1-3]. However, the eye height (EH) is only 1/3 of CD-NRZ [4], leading to a degraded SNR. PAM-4 further degrades the eye margin due to switching jitter (SWJ) [5] and complicates CDR [6]. On the other hand, simultaneous bidirectional signaling (SBD) enables simpler CDR and is free from SWJ [7], when using NRZ. However, in RC-dominant channels (e.g., silicon interposers for D2D), the R component causes resistive voltage division, making the inbound (IB) signal markedly smaller than the outbound (OB) signal [8], thereby resulting in harsher self-interference. Furthermore, SBD requires additional EQ and is vulnerable to mismatch between the replica and main driver [9].

In this work, capacitively driven simultaneous bidirectional signaling (CD-SBD) is proposed. CD-SBD delivers the same EH as CD-NRZ, while preserving the low driving power and EQ advantages of capacitive driving. In addition, the OB and IB amplitudes remain equal, since the swing size is determined by the capacitive ratio between driver and channel, rather than by resistive voltage division. The ease of CDR in SBD is also preserved. Nevertheless, the inherent replica mismatch issue of SBD still remains, especially under PVT variations. Figure 8.8.1(bottom left) shows the frequency-dependent mismatch [10] that arises between the main and replica driver. Prior works attempted to address this, but were limited by PVT variations. Reference [8] suffers from both self-interference and PVT. Reference [12] enhances SBD signal integrity, but at the cost of huge hardware overhead. An SBD mismatch adaptation method has been suggested in [11], but it only adjusts gain magnitude and requires external sweeping, making it vulnerable to VT drift. In this paper, a CD-SBD transceiver with an AC/DC replica incorporating PVT/mismatch tracking is proposed. This work suggests to decompose the mismatch into AC (i.e., high-frequency) and DC (i.e., low-to-mid frequency) components. That is, rather than using a single replica and dummy RC, the OB signal is reproduced by combining AC and DC replicas. Proposed edge-sample-based PVT/mismatch tracking enables real-time adaptation of those two weights (Wac, Wdc in Fig. 8.8.1) under VT drift. This enables: (i) good power efficiency by employing CD-SBD and removing dummy RC, (ii) PVT/mismatch tolerance by adapting AC/DC swings in background, and (iii) no additional hardware cost, as it reuses edge data for per-lane CDR.

Figure 8.8.2(top) shows the overall architecture of the proposed 56Gb/s/wire CD-SBD transceiver. The AFE integrates a capacitive driver, AC/DC replica paths, and a hybrid circuit that subtracts the AC/DC replica signal and a crosstalk cancellation (XTC) signal. Each of the 8 data channels incorporates a per-lane CDR, whose information is also used to track AC/DC mismatch. Two clock-forwarding channels are implemented, one per direction, with the clock driven capacitively as data and received via a TIA. In addition to the global CDR, a DLL-based quadrature generator is employed, incorporating a quadrature-error corrector (QEC) and duty-cycle corrector (DCC) with a quadrature-phase detector (QPD). Figure 8.8.2(left) shows the circuit implementation of the AC/DC replica, and corresponding hybrid circuit with XTC. In the replica path, a small inverter delivers a DC signal, while a small MOSCAP extracts the AC components. With peak-to-peak swing resolutions of about 5mV and 1.5mV, the AC/DC replicas are designed to cover gains of about 19dB and 16dB, respectively. Besides subtracting the emulated AC/DC components of the OB signal, the hybrid circuit also cancels out the crosstalk from 2 adjacent channels. Unlike the band-pass behavior in resistively driven interconnects, crosstalk (XT) in CD exhibits a low-pass nature [13]. To mimic the low-pass filtered XT signal, the XTC signal is constructed from the SBD - AC of the two adjacent channels. Since IB is already attenuated through the channel, it inherently resembles the low-pass filtered XT signal. Figure 8.8.2 (bottom) shows how the CD-SBD signal is composed of IB, OB, and XT components, and is restored by removing the XTC, AC, and DC components.

Figure 8.8.3 illustrates the operation of PVT/mismatch tracking. While conventional edge-sample-based CDR uses only edge and IB data, proposed tracking also utilizes OB data that is already known. Figure 8.8.3(top left) shows the case with a DC mismatch. If the replica DC weight is set too large so that '11' DC components are over-subtracted in the hybrid compared to the actual OB signal, the IB transition edge is pulled toward '0'. Thus, the edge is sampled as '0'. Conversely, if the replica DC weight is set too small and the '11' DC component is under-subtracted, the IB edge is pulled toward '1', and is sampled as '1'. That is, DC mismatch can be tracked using the edge data when the OB data is either '00' or '11'. Similarly, Fig. 8.8.3(bottom left) shows the case with an AC mismatch. When the OB data is '01', an over-estimated AC weight pulls the IB edge towards '0'. Conversely, when the OB data is '10', an over-estimated AC weight pulls the IB edge towards '1', and is sampled as '1'. Figure 8.8.3 (top right) shows the pattern filter table. While the per-lane CDR operates as convention using IB and edge data, the proposed CD-SBD additionally exploits the OB data to track AC/DC mismatch in the hybrid under PVT variation. Figure 8.8.3 (bottom right) compares the RC variation tolerance between the conventional and the proposed schemes. With conventional SBD using a replica and dummy RC, a -20% RC variation in the replica path reduces the eye height (EH) to about 40%. In contrast, the proposed CD-SBD with PVT/mismatch tracking restores EH to nearly 100% under the same condition.

Figure 8.8.4 illustrates the proposed DLL-based quadrature generator with QEC and DCC function. Since the clock is forwarded using a single lane in this work, it is crucial to correct duty cycle and quadrature error to ensure clock quality [14]. Figure 8.8.4(top) shows the block diagram of the quadrature generator and the circuit implementation of the QPD. The durations of Q1-Q4 in the timing diagram correlate with duty and quadrature errors as follows. If the quadrature delay is less than 90°, Q2 and Q4 increase while Q1 and Q3 decrease, and vice versa. Similarly, if the duty cycle modulated by DCC exceeds 50%, Q1 and Q2 increase while Q3 and Q4 decrease, and vice versa. Thus, the sign (+/-) of (Q2-Q3) + (Q4-Q1) indicates the quadrature error polarity, while the sign of (Q2-Q3) + (Q1-Q4) indicates the duty cycle error polarity. The proposed QPD converts (Q2-Q3) and (Q1-Q4) into complementary voltage pairs. Each quadrature interval (Q1-Q4) is translated into pull-up (PU) and pull-down (PD) currents, and the resulting charge is integrated onto the corresponding node (Fig. 8.8.4, top right). Thanks to the complementary PU/PD networks, PN mismatch is canceled between the two nodes, enabling accurate comparison of (Q2-Q3) and (Q1-Q4). Next, the comparators detect the sign of (Q2-Q3) + (Q4-Q1) and (Q2-Q3) + (Q1-Q4), thereby the quadrature phase error and the duty cycle error are precisely detected. The proposed DLL-based quadrature generator with QEC/DCC achieves <0.3% duty cycle error and 230fs quadrature phase error.

The prototype chip is fabricated in a 28nm CMOS process. Since real process variations and mismatch are difficult to quantify or reproduce across chips, intentional variations were introduced into 8 channels to explicitly demonstrate the effects of process variation and mismatch, as illustrated in Fig. 8.8.5 (top). Channels are configured as on-chip metal lines, and additional R and C are inserted in the middle of lanes 3-8 with various amounts to emulate process variation in RC-dominant channels for D2D interfaces [15]. These introduce up to 3dB of additional insertion loss. Furthermore, to realize mismatch between the main and replica drivers, additional R is inserted to the main drivers of the lane 2, 4, 6, and 8, resulting in 2dB of additional loss. All 8 channels are implemented with 2mm long, 0.4μm wide, and 1.8μm pitch. The baseline channel, without additional RC components or driver mismatch, exhibits an insertion loss of -6.5dB at the Nyquist frequency of 14GHz, while the worst-case channel shows an insertion loss of -11.5dB. The worst-case FEXT from adjacent channels is -18.2dB at Nyquist, for all 8 channels.

Figure 8.8.5 (bottom) shows the measured bathtub curves and eye diagram of the proposed transceiver. Bottom left illustrates the bathtub curves of CH0 when (i) CDR, PVT/mismatch tracking, and XTC are all disabled, (ii) only CDR and PVT/mismatch tracking are enabled, and (iii) all are enabled. When all are disabled, the eye margin is measured as 0UI at a BER of 10^{-12}, whereas enabling all improves it to 0.32UI. With PVT/mismatch tracking enabled, all channels exhibit BER below 10^{-12}. The bottom right shows the eye diagram of CH0, with the vertical and horizontal eye margin of 84mV and 0.56UI, respectively, at a BER of 10^{-12}.

Figure 8.8.6 presents the measured performance of PVT/mismatch tracking under process variation, voltage drift, and temperature drift, respectively. To evaluate process variation tracking, CDR and PVT/mismatch tracking were applied in CH0 and, using the same parameters, the eye diagram was measured in CH3, where process variation was emulated by clock skew, driver mismatch, and RC variation with different channel loss. Without CDR and tracking, the optimum sampling point deviates by ~0.25UI, with the vertical and horizontal eye margin of 28mV and 0.16UI, respectively, although BER at the sampling point

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is unmeasurable. With CDR and tracking enabled, the sampling point is restored to the optimum position, and the eye margin improves to 80mV and 0.28UI. Similarly, when supply voltage (VDDA, VDDQ) drifts from 1.0V to 0.93V, the eye shifts by ~0.5UI, and the voltage margin reduces to 24mV. After applying CDR and tracking, the eye margin recovers to 64mV and 0.28UI. Figure 8.8.6(right) shows the measured eye height and eye width under supply voltage variation from 0.93V to 1.2V, and ambient temperature variation from 0 to 80°C. Figure 8.8.7 summarizes the TRX performance compared with other state-of-the-art D2D TRXs. Per-lane CDR and PVT/mismatch tracking incur 15.6% area and (α × 16.8)% power overhead, where α denotes the adjustable CDR loop active factor used to save power for low-frequency VT tracking. The area and power overhead of the proposed tracking itself is negligible. This work demonstrates PVT-variation tolerance and apower efficiency of 0.292pJ/b by proposing: (i) CD-SBD with (ii) AC/DC hybrid, (iii) PVT/mismatch tracking, and (iv) DLL-based quad-gen. The die photograph shows the active area of 0.01697mm^2.

Acknowledgement:
This work was supported in part by Samsung Electronics Co., Ltd., and by Institute of Information & communications Technology Planning & Evaluation (IITP) under the artificial intelligence semiconductor support program to nurture the best talents (IITP-2025-RS-2023-00256081) grant funded by the Korea government(MSIT). The EDA tool was supported by the IC Design Education Center(IDEC), Korea. Woo-Seok Choi (wooseokchoi@snu.ac.kr) is the corresponding author.

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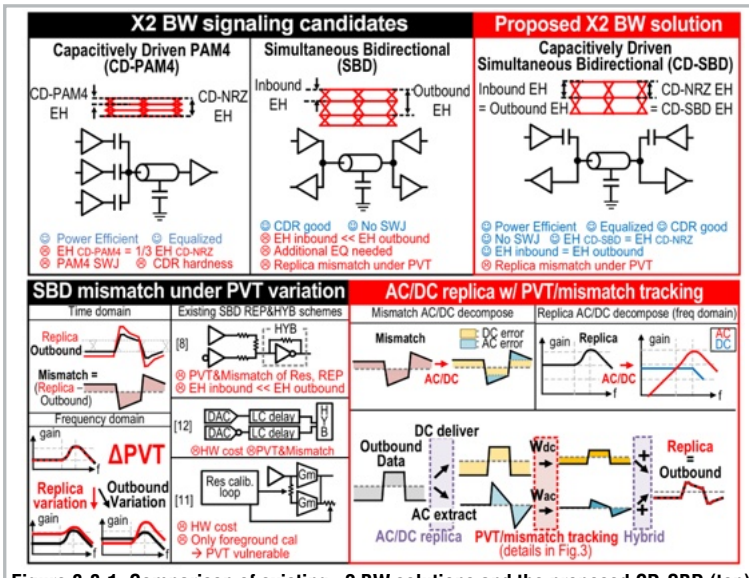


Figure 8.8.1: Comparison of existing ×2 BW solutions and the proposed CD-SBD (top); replica mismatch problem of SBD under PVT variation and the proposed AC/DC replica with PVT/mismatch tracking (bottom).

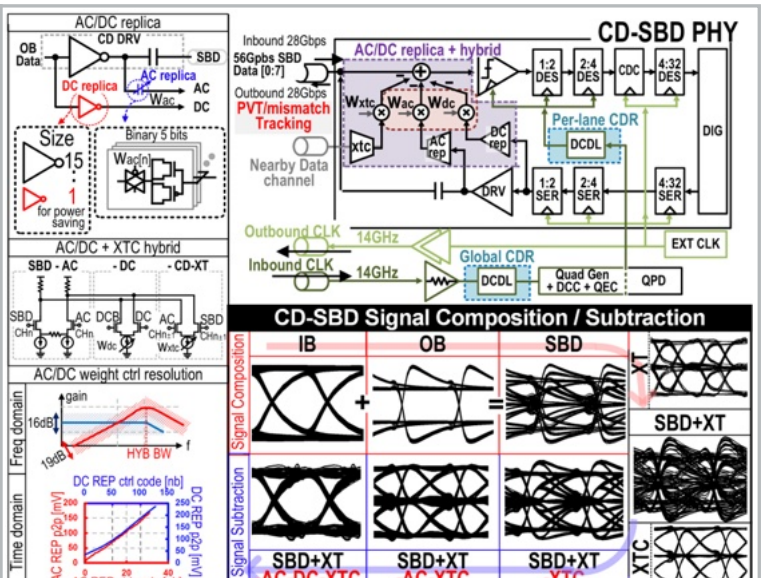


Figure 8.8.2: Proposed CD-SBD TRX (top right); circuit implementation of the AC/DC replica and hybrid (left); signal composition/subtraction principle in CD-SBD (bottom).

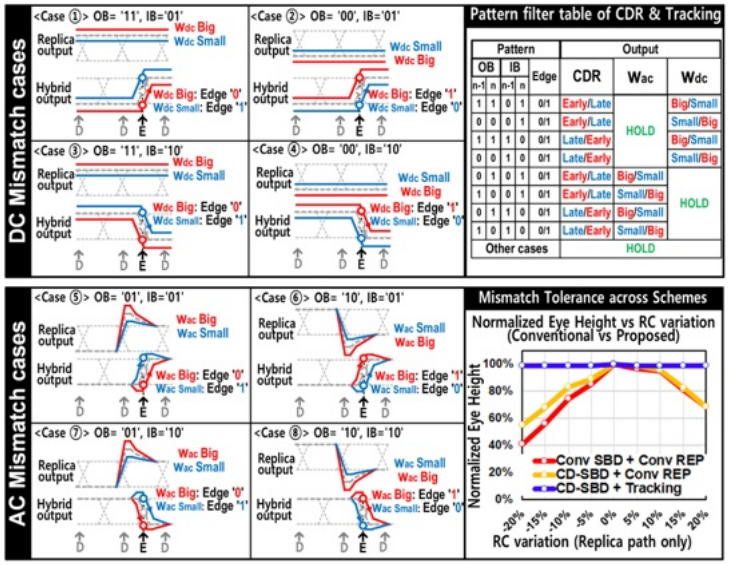


Figure 8.8.3: Operating principle of the proposed PVT/Mismatch tracking: DC mismatch cases (top left), AC mismatch cases (bottom left), pattern filter table (top right) and comparison of mismatch tolerance.

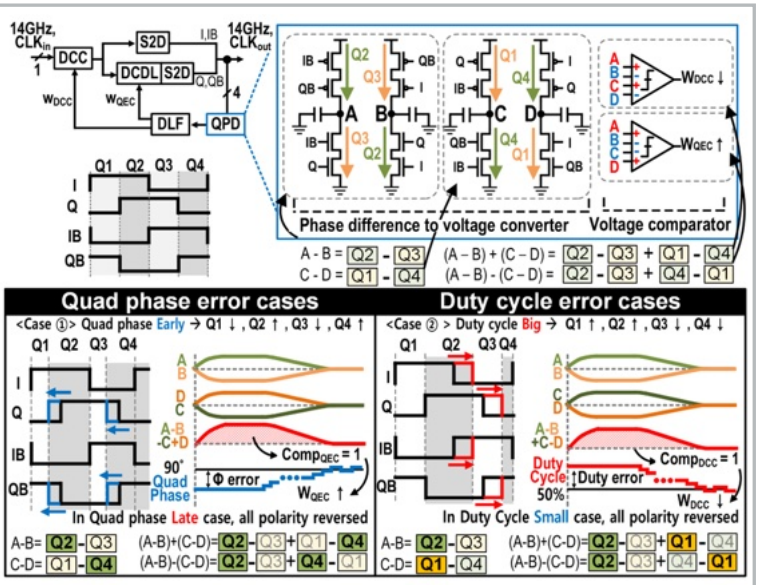
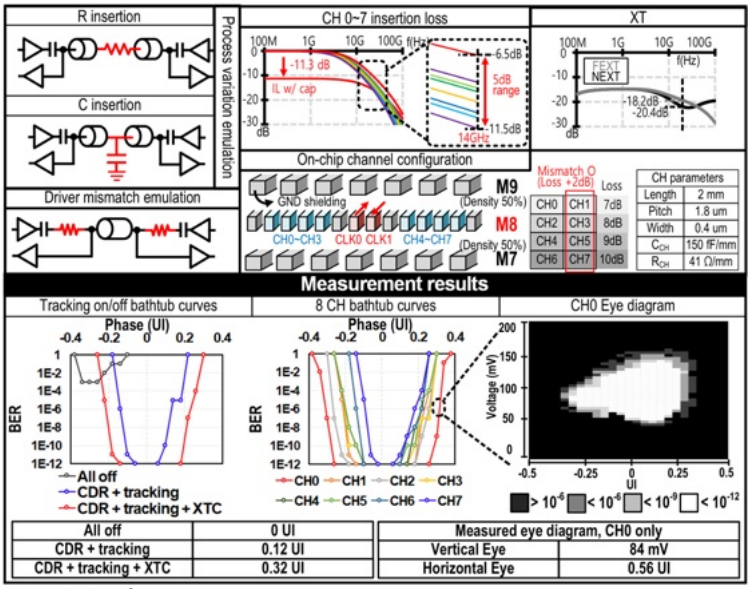


Figure 8.8.4: Proposed quadrature generator with QEC/DCC: block diagram (top left), circuit implementation of QPD (top right), error detection in QEC/DCC (bottom).



All off	0 UI
CDR + tracking	0.12 UI
CDR + tracking + XTC	0.32 UI

Measured eye diagram, CH0 only	
Vertical Eye	84 mV
Horizontal Eye	0.56 UI

Figure 8.8.5: Channel setup with injected mismatch, process, channel loss variation and channel parameters (top); measured BER bathtub curves and eye diagram.

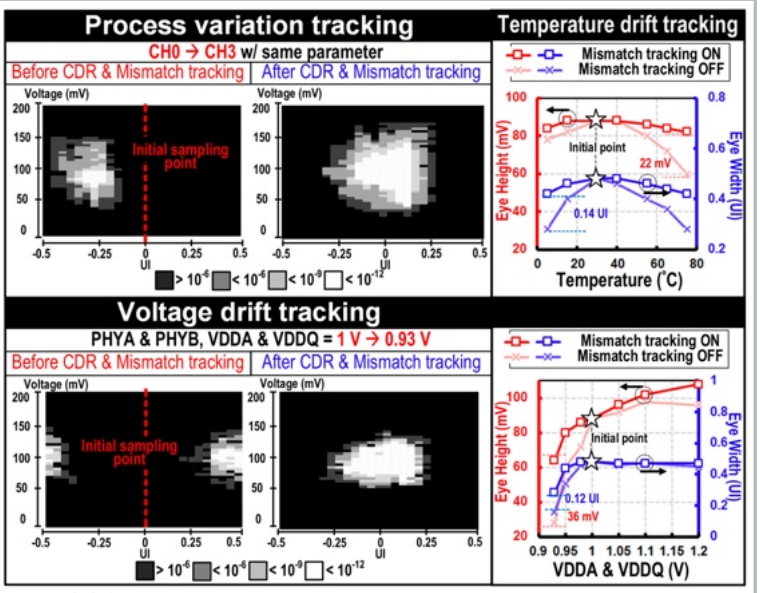
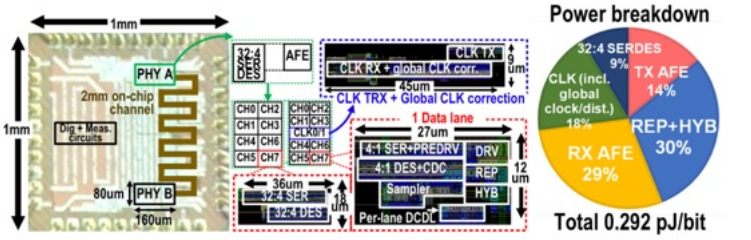


Figure 8.8.6: Measured eye diagrams and tolerance under process, voltage, and temperature variations.



		JSSC'23[8]	ISSCC'25[16]	JSSC'25[17]	ISSCC'24[18]	JSSC'24[4]	This work
Technology		5nm FinFET	28nm CMOS	3nm FinFET	4nm FinFET	28nm CMOS	28nm CMOS
Data rate (Gb/s/pin)		50.4	64	32	48	24	56
Signaling		SBD	SBD	NRZ	NRZ	CD-PAM4	CD-SBD
Channel Loss @ Nyq. Freq. [dB]		-5.4	-2.8	-2.4	-3	-4.3	-6.5 ~ -11.5
PVT variation tracking	CLK skew	X	X	O	X	X	Per-lane CDR, QEC+DCC+4ϕgen AC/DC replica w/ PVT/Mismatch tracking
	Data mismatch	X	X	X	X	X	
XTC		X	O	X	X	O	O
Area (μm²)		11326*	11820*	7000	67833	1010	1697.5**
Energy efficiency (pJ/bit)		0.297	1.21	0.36	0.67	0.458	0.292***

* per-lane area including 2 PHY for SBD
** per-lane active area of 8 data & 2 clock lanes, including 2 PHY for SBD.
Calculated by dividing the total active area (including global clock & 2 clock TRX lanes, excluding dig) by 8 data lanes.
*** per-lane power of 8 data & 2 clock lanes, including 2 PHYs for SBD.
Calculated by dividing the total PHY power (including global clock & 2 clock TRX lanes, excluding dig) by 8 data lanes.

Figure 8.8.7: Chip microphotograph, power breakdown and comparison table.

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