5.7 A 29nW Bandgap Reference Circuit

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Bandgap references (BGRs) are widely used to generate a temperature-insensitive reference voltage determined by the silicon bandgap. The BGR generally utilizes PN diodes to generate both of proportional-to-absolute-temperature (PTAT) and complementary-to-absolute-temperature (CTAT) quantities and combines them to eliminate the temperature dependency. Though the BGR provides a robust voltage or current reference with insensitivity to process, voltage and temperature variations that is superior to CMOS-only reference circuits, it has received little attention in ultra-low-power (ULP) sensor applications. While CMOS-only reference circuits have recently demonstrated nanowatt power consumption [1], BGR approaches still have two critical factors to preventing nanowatt consumption. One is that PTAT generation assumes sufficient forward bias, VD, of the PN junction to allow $e^{VD/(n\text{-}VT)}$ to be much larger than 1 in the temperature range of interest, where n and VT (=kT/q) represent the ideality factor and the thermal voltage, respectively. In addition, the PTAT generation requires a start-up circuit to prevent the circuit from resting at the undesirable zero-bias condition. Since the start-up circuit utilizes a resistive voltage division between power rails, it consumes non-zero DC current, which must be larger than leakage current in order to ensure stable start-up operation. These two requirements for PTAT generation limit the use of BGRs in nanowatt ULP applications.

Recently, a sample-and-hold scheme with duty cycling was applied to a BGR circuit and achieved a power consumption of a few nanowatts [2]. However, it uses a traditional BGR core and does not reduce the power consumption of the BGR circuit itself when it is turned on. Therefore, further reduction of power consumption would be achieved if a similar sample-and-hold scheme were applied to a more energy-efficient BGR core. It also requires a large silicon area to implement sampling capacitors. Resistor-less PTAT schemes with cascaded source-coupled pairs have been another approach to achieve sub-μW BGRs [3,4]. However, these suffer from degraded performance in temperature sensitivity and line regulation due to increased dependency on transistor characteristics.

This paper proposes a BGR with a leakage based PTAT. Without any start-up circuit, duty-cycling, or assumption of strong forward bias for the PTAT, the fabricated BGR in 0.35μm CMOS consumes 29nW at room temperature and shows a temperature coefficient of 12.75ppm/°C with a line regulation of 0.198%/V. Figure 5.7.1 shows the proposed concept of two-diode PTAT generation. The two diodes are identical except for a multiplication factor, L, determined by the ratio of the numbers of identical diodes used at pull-up and pull-down sides. The diodes are connected in series between power rails with the upper diode reverse biased. Then, only leakage current, $L \cdot Is$, flows through the branch, where *Is* represents the reverse saturation current. The intermediate node voltage becomes PTAT, $nV_T\ln(L+1)$, without the assumption of enough forward bias of the lower diode to guarantee that $e^{VD/(n\text{-}VT)}$ is much larger than 1. In addition, since this circuit utilizes the leakage current, which always flows, there is no need of a start-up circuit. Therefore, the proposed scheme dramatically reduces the current consumption for PTAT generation which has been a major cause of power consumption in the conventional BGR. This concept of two-diode PTAT generation can be also extended to use other diodes if they are identical. Replacement of PN diodes with MOS diodes also results in PTAT generation. The MOS current equation in the sub-threshold region is $I_{sub}=\mu C_{ox}(W/L)(m-1)V_T^2\exp((V_{gs}-V_{th})/mV_T)(1-\exp(-V_{ds})/V_T)$, where m is the inverse of the gate-to-surface coupling coefficient. The intermediate node voltage can be derived to be $mV_T\ln(L)$, resulting in a PTAT voltage. Recently, this MOS version of PTAT generation was adopted in the design of a temperature sensor [5]. This work generalizes the design of the PTAT with two identical diodes and extends it to form an ultra-low-power BGR circuit.

Note that conventional BGR circuits take the diode voltage for CTAT while the difference between two CTATs becomes PTAT. In the proposed scheme, the PTAT is directly taken from the diode voltage. Therefore, the current for PTAT generation increases exponentially as temperature changes and could range from fA to nA. The PTAT generated by drawing too little current at low temperatures can be affected by unwanted gate leakage current from circuits to be connected to the PTAT node because the gate leakage has less dependence on temperature. Simulated current for PTAT generation is shown in Fig. 5.7.1. Assuming that the two versions are implemented in the same area, the PN diode and MOS diode versions consume 30fA and 60pA at room temperature, respectively, while they consume 2nA and 13nA at 120°C. The larger current variation in the PN version is due to stronger temperature dependency of *Is*. In this work, the MOS diode version is used considering the layout area and reasonable current level, which should be much larger than the gate leakage current given by the process technology.

Figure 5.7.2 shows the circuit schematic of the proposed BGR. The PTAT voltage is copied by an opamp, drawing PTAT current through resistors. The opamp has a source-follower-based level shifter followed by an NMOS differential pair at the input stage to receive low PTAT voltage. Total current consumption for the opamp is less than 1nA at room temperature. The total power consumption of the BGR is dominated (> 99% at room temperature) by the current through resistors, and can be reduced by increasing the resistance at the cost of area. A lateral NPN BJT (Fig. 5.7.3) with twin-well technology is stacked on the resistors to implement a PN diode, providing a CTAT voltage. The voltage reference, Vref, can be derived as $(1+R_2/R_1)V_{PTAT}+V_{CTAT}$, eliminating the temperature dependency by adjustment of the ratio between R_1 and R_2.

The designed BGR circuit is fabricated using a 0.35μm CMOS process. The measured temperature coefficient (TC) is 12.75ppm/C when temperature changes from -10°C to 110°C. Figure 5.7.4 shows measured reference voltages from 10 chips. The standard deviation is 2.36mV at 20°C, revealing a μ/σ of 0.2%. Figure 5.7.5 shows the measured reference voltage when supply voltage varies. The reference voltage increases by 2.3mV as the supply voltage increases by 1V, showing a line regulation of 0.198%/V. Current consumption is also measured as temperature changes. The total current linearly increases up to 60°C, revealing that the current through the resistors is dominant while the leakage current for PTAT generation and opamp operation is negligible. The BGR circuit consumes 28.7nW from a 1.4V supply voltage at room temperature. Above 60°C, the exponentially increasing leakage current starts to appear as a comparable contributor to the total power consumption. Figure 5.7.6 summarizes the performance and compares it with previously reported state-of-the-art BGR circuits.

Acknowledgements:
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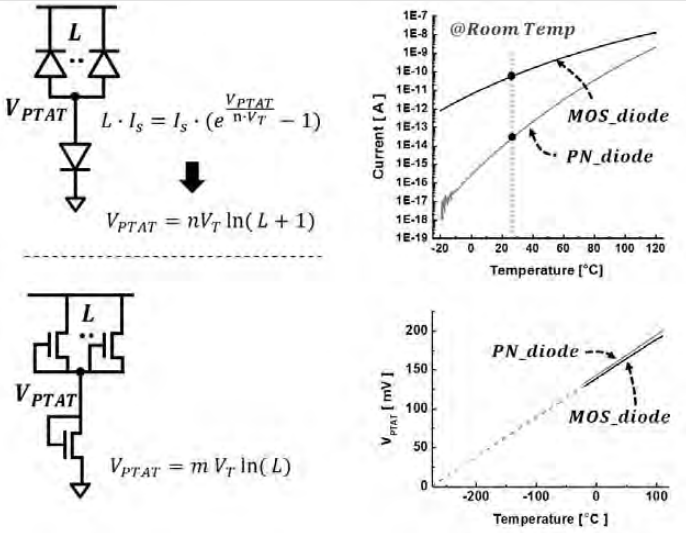

Figure 5.7.1: Proposed concept of two-diode PTAT generation using leakage current.

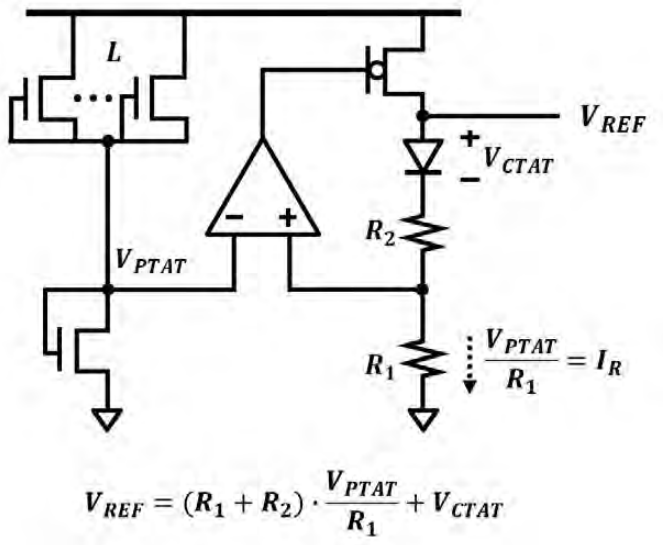

Figure 5.7.2: Proposed bandgap voltage reference circuit.

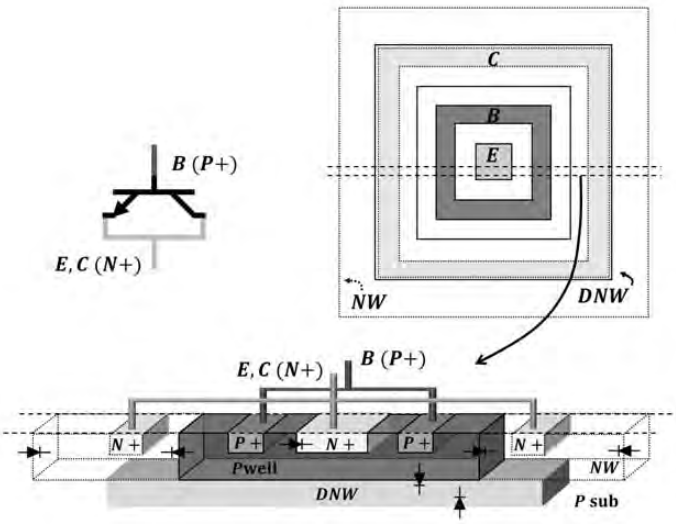

Figure 5.7.3: Structure of lateral NPN BJT for CTAT.

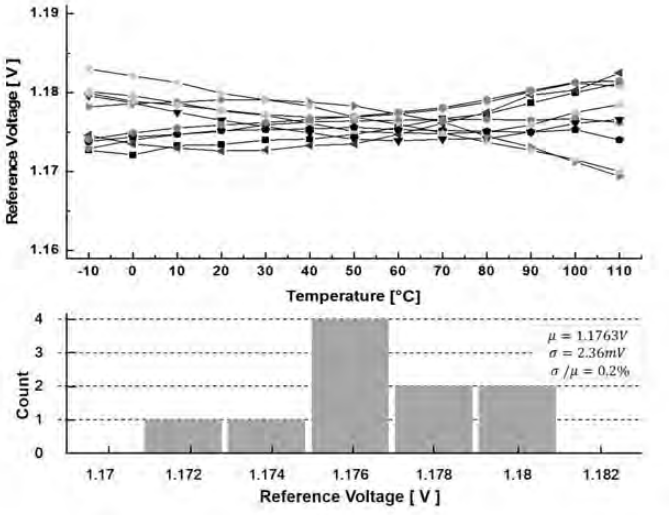

Figure 5.7.4: Measured reference voltage from 10 chips and distribution of the reference voltages at 20°C.

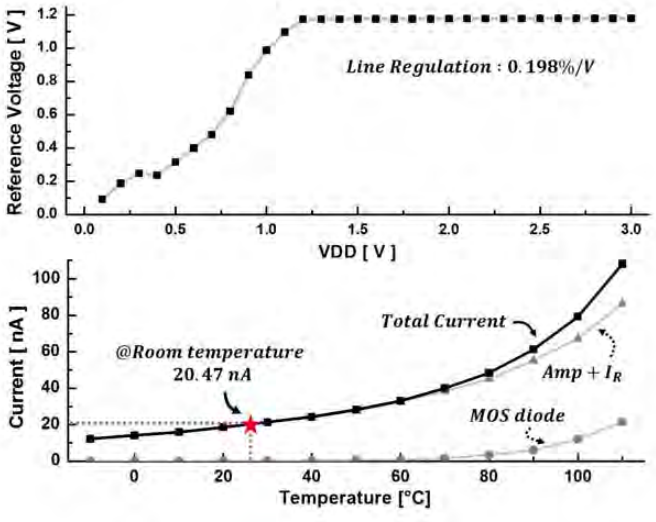

Figure 5.7.5: Measured line regulation and current consumption.

	This Work	[3] JSSC 13	[4] ASSC 10	[6] JSSC 07	[7] JSSC 11	[8] JSSC 02
Power [W]	**28.7n @R**	100n @R	108n @N/A	162u @R	99u @N/A	1.4m @N/A
TC [ppm/C°]	12.75	147	215	12.4	5-12	120
Active Area [mm²]	0.48	0.0294	0.21	1.2	0.12	0.4
σ/μ [%]	0.2	0.737	1.61	N/A	0.15	N/A
LR [%/V]	0.198	N/A	0.45	N/A	N/A	N/A
Temp Range [C°]	-10 ~ 110	-40 ~ 120	-20 ~ 80	-20 ~ 100	-40 ~ 125	0 ~ 70
Output [V]	1.176	1.09	1.18	0.858	1.09	1.12
Tech [μm]	0.35	0.18	0.35	0.35	0.16	0.5
Type	BGR	BGR	BGR	Sub-BGR	BGR	BGR

Figure 5.7.6: Performance summary and comparison with previous works.

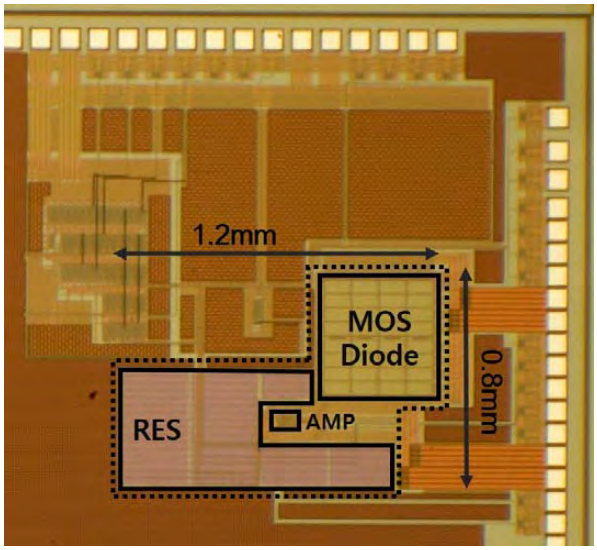

Figure 5.7.7: Chip micrograph.

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