5.5 A Forward-Body-Bias Tuned 450MHz Gm-C 3rd-Order Low-Pass Filter in 28nm UTBB FD-SOI with >1dBVp IIP3 over a 0.7-to-1V Supply

Joeri Lechevallier[1,2], Remko Struiksma[1], Hani Sherry[2], Andreia Cathelin[2], Eric Klumperink[1], Bram Nauta[1]

[1]University of Twente, Enschede, The Netherlands,
[2]STMicroelectronics, Crolles, France

Due to the absence of internal nodes, inverter-based Gm-C filters [1,2] allow achieving bandwidths beyond what is possible with opamp-RC techniques. The class-AB behavior of the inverter, together with the high transconductance for a given quiescent current, results in a high dynamic range for a given power consumption when optimally biased [3]. The major disadvantage of traditional inverter-based Gm-C filters is that they are tuned with the supply voltage, V_{DD}, and hence require a finely controllable supply. Voltage regulators used to accomplish this require a voltage headroom (including margin for tuning) and degrade total power efficiency by tens of percent. In this paper, we show that by exploiting body biasing in an ultra-thin buried oxide (BOX) and body, fully-depleted SOI (UTBB FD-SOI) CMOS technology, we overcome the requirement for a tunable V_{DD} in inverter-based Gm-C filters, while achieving high linearity over a wide supply voltage range.

A cross-section of an UTBB FD-SOI CMOS inverter is shown in Fig. 5.5.1 [4]. The BOX underneath the active devices isolates the drains and sources from the bulk, allowing the transistor body to be used as a back-gate, hence enabling significant threshold voltage (V_t) shifts. Low-V_t (LVT) devices in this technology are implemented as 'flip-well' transistors, where the NMOS and PMOS devices lay above n- and p-wells, respectively. Due to the BOX isolation, there are no drain- and source-to-bulk parasitic diodes, which limit the maximum forward body bias (FBB) range in bulk technology. For 28nm UTBB FD-SOI LVT transistors, a FBB of up to 3V is allowed. Combined with a higher sensitivity to the body bias (85mV/V in UTBB FD-SOI vs. 25mV/V in bulk), this allows V_t to be varied by approximately 250mV, much more than the tens of mV in bulk technologies. This directly implies that the sum of the overdrive voltages of NMOS and PMOS devices can be kept constant over hundreds of mV supply range, hence compensating for supply voltage variations. Alternatively, FBB can be used to tune the transconductors. Body biasing requires negligible current (<1nA), consisting only of leakage currents of reverse-biased diodes.

Illustrated in the bottom left plot of Fig. 5.5.1 is the change in the Gm curve of a differential CMOS inverter over V_{DD} variations. Without body biasing, Gm changes and linearity is degraded. For high V_{DD}, the inverter behavior is compressive (mobility reduction), while for low V_{DD} it is expansive (exponential region). Only one V_{DD} results in a flat Gm-curve, which means that it produces little 3rd-order distortion. Body biasing can be applied to tune Gm back to its nominal value over different V_{DD}, without linearity degradation, as illustrated in the bottom right plot of Fig. 5.5.1. We apply this technique to a low-pass (LP) Gm-C filter to keep the cut-off frequency (Fc) constant and to guarantee high linearity over a 300mV supply voltage range. Local supply decoupling is still required, but the separate voltage regulator can be omitted. Without this technique, the same supply variation would have shifted the cut-off frequency between 110 and 650MHz and degraded IIP3 by more than 10dB.

The LP filter topology shown in Fig. 5.5.2 is derived from a 3rd-order, doubly terminated Butterworth LC ladder prototype using gyrator synthesis [1]. The transconductors and MOM capacitors are sized for a nominal Fc of 450MHz. The use of 110nm gate lengths in 28nm UTBB FD-SOI technology makes the transconductor output resistance sufficiently constant to be compensated by a fixed negative resistance, eliminating the need for Q-tuning as used in previous designs [1,2,5]. The increased MOSFET parasitic capacitances are absorbed in the filter capacitances. The common-mode loop gain must be kept below unity, which is accomplished by inverters gm_b and gm_c [1]. We choose gm_b=0.350gm_a and gm_c=0.325gm_a to minimize noise and power consumption, while still ensuring common-mode stability and output resistance cancellation [2].

As shown in Fig. 5.5.2, all NMOS and PMOS devices are body biased by VBBN (biased from 0 to 3V) and VBBP (biased from 0 to -3V) respectively. Impedance up-scaling by a factor of 2 is applied to the last nodes (N3) to achieve unity gain overall, while reducing power consumption. To measure the filter in a 50Ω environment, inverter buffers are added at the filter output, and 50Ω resistors terminate the input and output. A reference path is integrated on chip to enable de-embedding of the filter core [1]. The chip, of which a micrograph is shown in Fig. 5.5.7, is integrated in STMicroelectronics 28nm UTBB FD-SOI technology. The filter core occupies 0.04mm^2, of which 0.03mm^2 are filter capacitors.

The S-parameters of the filter path, reference path and PCB crosstalk were measured, from which the transfer function of the filter core was de-embedded. Using FBB tuning, the filter Fc is kept constant at 450MHz for a V_{DD} varying from 0.7 to 1V. Figure 5.5.3 shows the measured filter transfer function. This figure also shows another tuning strategy where V_{DD} is fixed at 0.9V, and Fc is varied between 190MHz and 900MHz using FBB tuning between 0 and 3V.

The 3rd-order intermodulation distortion of the filter path, including output buffers, is measured with 2 in-band tones at 300±0.5MHz. Figure 5.5.4 shows the IIP3 for different V_{DD}, where VBBP and VBBN are varied, showing that the IIP3 can be maximized for every supply level. Figure 5.5.5 shows the IM3 and fundamental against input power when Fc is tuned to 450MHz, for different V_{DD} values. These curves extrapolate to an IIP3 above 1.2dBVp. The 1dB compression point was measured by sweeping the power of a single 300MHz tone, and varies between -10.3 and -4.8dBVp. The input noise power spectral density (PSD) of the de-embedded filter core is approximately 6nV/√Hz, and power consumption varies between 4mW and 5.6mW over the 0.7–1V supply range.

The filter performance is summarized and compared to four other recent Gm-C filters with a cut-off frequency above 100MHz in Fig. 5.5.6. Three key performance figures (noise, linearity and power consumption) can be easily traded against each other; the noise PSD can be reduced by impedance scaling at the expense of a proportional increase in power consumption [3], while linearity can be improved at the expense of noise by attenuating the input, keeping the dynamic range the same. To allow comparison of the different circuits, taking these design freedoms into account, we calculate their normalized signal-to-noise ratio (NSNR) in the last row of Fig. 5.5.6 [3]. Compared to previous work this design achieves either a higher linearity, or a lower noise level and lower power consumption. Compared to the most similar filter in [2] this work obtains over 3dB higher SFDR at lower power consumption, while not needing a regulated supply. The SFDR of this design is 3dB lower than [7], yet consumes 12 times less power. This performance is maintained over a 0.7–1V supply range.

This paper has demonstrated that the extended body biasing range in UTBB FD-SOI, applied to an inverter-based Gm-C filter, can save a significant amount of power while accommodating supply voltage variations, without performance degradation and with competitive linearity.

Acknowledgments:
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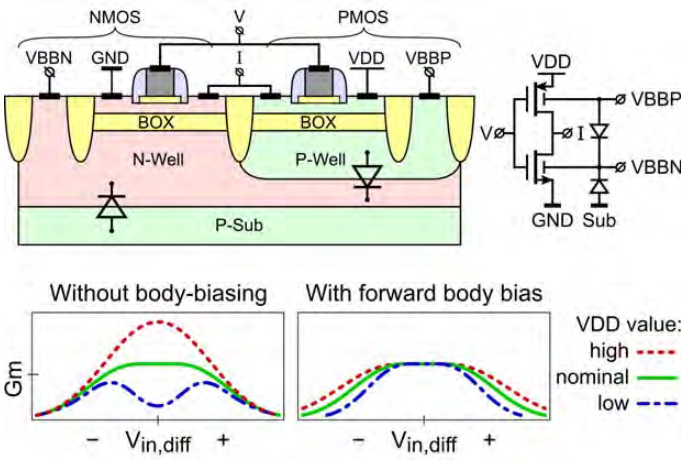

Figure 5.5.1: Inverter cross section with typical Gm curves.

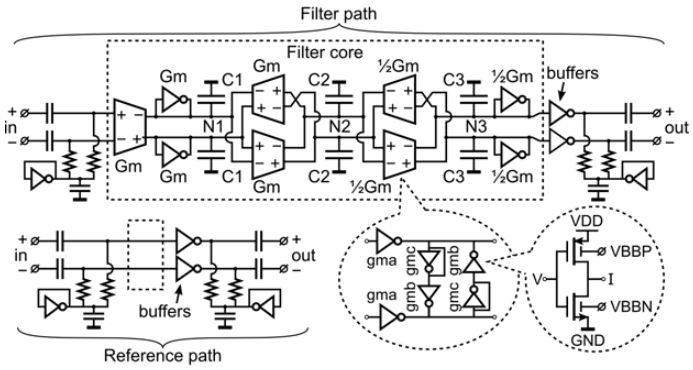

Figure 5.5.2: Chip schematic.

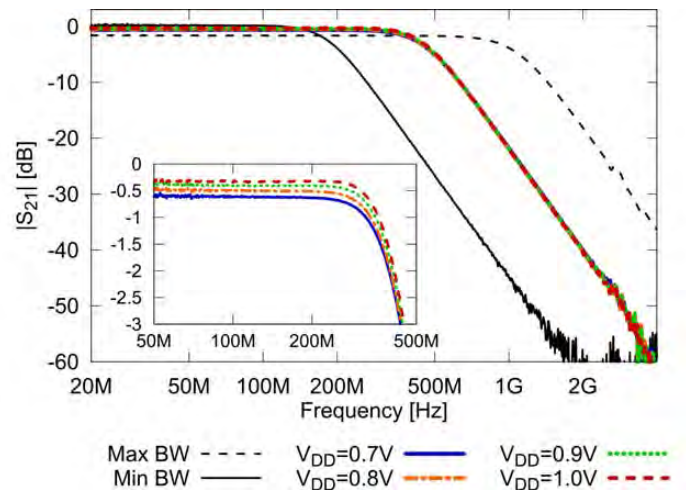

Figure 5.5.3: De-embedded transfer function.

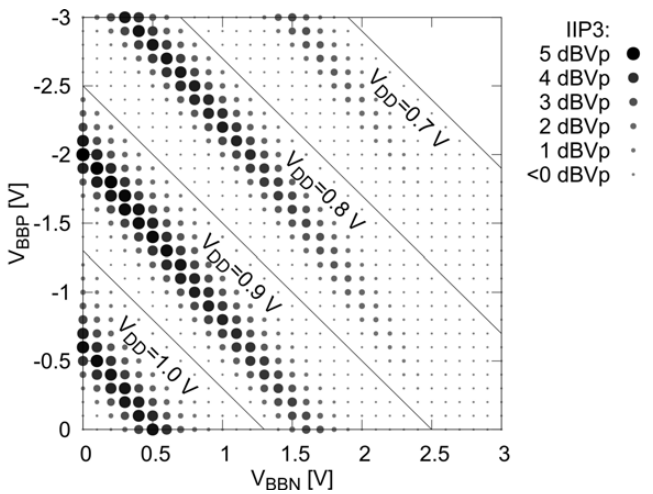

Figure 5.5.4: IIP3 versus forward body bias, for different supplies.

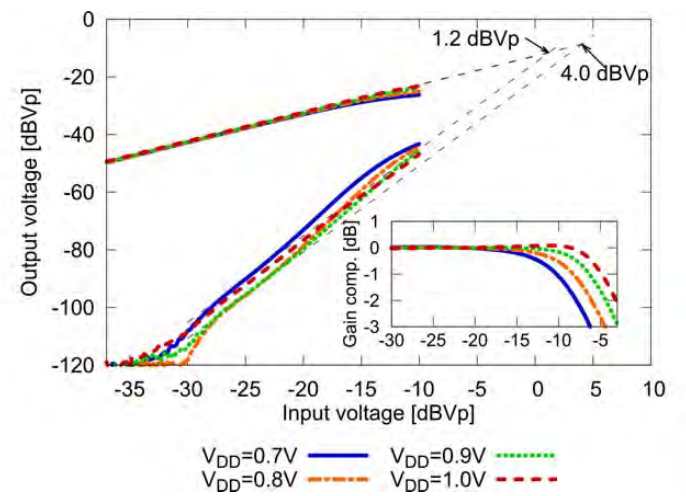

Figure 5.5.5: IIP3 and gain compression.

	This work				[2]	[5]	[6]	[7]
Technology	28nm FD-SOI CMOS				65nm CMOS	65nm CMOS	0.13um CMOS	0.18um CMOS
Order	3				3	5	2	3
Type	Butterworth				Chebychev			Elliptic
Supply voltage [V]	0.7	0.8	0.9	1	1	1.2	1.2	1.8
Cut-off freq. [MHz]	454	454	457	459	4700	275	200	300
In-band gain [dB]	-0.7	-0.6	-0.5	-0.3	2.7	9	0	0
Inp. ref. noise [$nV_{rms}/\sqrt{Hz}$][a]	5.9	6.1	6.1	5.9	6.61	7.8	35.4	5
in-band IIP3 [dBVp][a]	1.2	4.0	4.0	2.4	-3	-12.5	4	6.9
1dB comp. [dBVp]	-10.3	-8.2	-6.3	-4.8	—	—	—	—
Power diss. [mW]	4.0	4.6	5.2	5.6	19 [c]	36	20.8	72
Filter area [mm^2]	0.04 (core: 0.01,caps: 0.03)				0.01	0.21	0.5	0.9
SFDR/BW [dB/Hz]	108.5	110.2	110.2	109.3	105.1	97.8	100.0	113.3
NSNR [dB][b]	136.7	138.7	138.2	136.5	124.8	111.1	116.8	131.3

[a] Calculated assuming 50Ω matching

[b] NSNR = SNR/P normalized to 1mW, 1Hz bandwidth and 1% IM3 [3]

[c] Excluding voltage headroom for tuning

Figure 5.5.6: Performance summary and comparison.

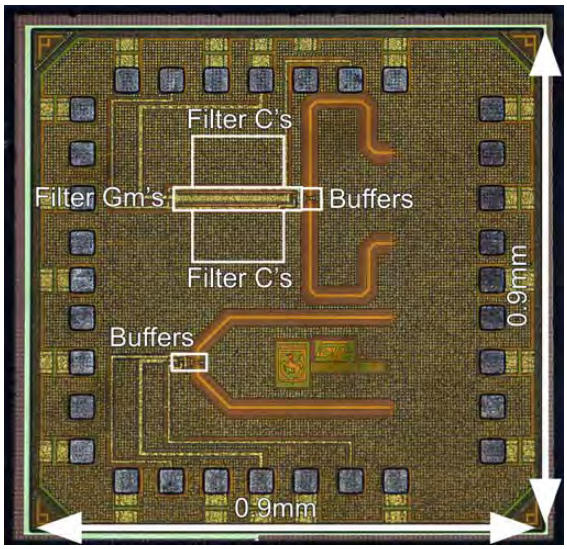

Figure 5.5.7: Chip micrograph.

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