5.4 A 32nW Bandgap Reference Voltage Operational from 0.5V Supply for Ultra-Low Power Systems

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Most systems require a voltage reference independent of variation of power supply, process, or temperature, and a bandgap voltage reference (BGR) often serves this purpose. For ultra-low power (ULP) systems, the BGR may constitute a significant component of standby power, and the system start-up voltage is often determined by the voltage, V_{in}, at which the BGR becomes operational. Lowering V_{in} can also allow an ULP system to continue operation longer as its battery or energy harvested input voltage decreases. The minimum V_{in} for state-of-the-art BGRs is restricted by $V_{EB}+V_{DS}$ [1], where V_{EB} is the emitter-base voltage of a *pnp* transistor, and V_{DS} is the drain-source saturation voltage of a MOS transistor. Recent work brings the V_{in} voltage down to 700mV [2]. There is a need to reduce the standby power and V_{in} of a BGR to increase the lifetime of ULP systems. This paper presents a BGR circuit with measured minimum operating V_{in} of 500mV, reducing the V_{in} of [2] by 1.4×. Further, the power consumption of the proposed circuit is 32nW, which is 1.6× lower than the non-duty cycled BGR reported in [2]. A 2×-charge pump based bandgap core, a switched-capacitor network (SCN), and a current controlled oscillator and clock doubler circuit enable a BGR with a temperature variation of 75ppm/°C and power supply rejection (PSR) of up to -52dB at DC.

Figure 5.4.1 shows the circuit diagram of the proposed BGR comprising 2× charge pump cells, BJT transistors Q_1 and Q_2, capacitors C_{fx} and C_{Lx}, and a SCN to generate V_{REF}. The output of one 2× charge-pump cell drives Q_1 and C_{L1}. In the absence of Q_1, C_{L1} will charge to $2V_{in}$, but Q_1 clamps the output voltage to V_{EB1}, which is complementary to absolute temperature (CTAT). Similarly, V_{EB2} is generated using Q_2 and C_{L2}, where Q_2 is M times Q_1. The difference in voltage between V_{EB1} and V_{EB2} is ΔV_{BE}, which is proportional to absolute temperature (PTAT) and is stored on C_Δ (Fig. 5.4.1). The SCN scales V_{EB} and ΔV_{BE} by constants *a* and *b* to generate the temperature independent BGR voltage, V_{REF} (Fig. 5.4.1). The charge pump circuit configuration with the BJT enables the low voltage operation of the BGR. The minimum V_{in} required to generate V_{EB} and ΔV_{BE} is $V_{EB}/2$ in the circuit of Fig. 5.4.1, which is approximately 375mV, 2× lower than [3].

Figure 5.4.2 shows the switched-capacitor network (SCN) of the BGR circuit. It generates constants for scaling V_{EB} and ΔV_{BE} and then generates V_{REF} using non-overlapping phases of the clock (CLK), φ_1 and φ_2. In phase φ_2 (Fig. 5.4.2), C_{a1} is discharged to ground while the top plates of C_{a2}, C_{b1}, C_{b2}, and C_{b3} are connected to V_{EB1}. The bottom plate of C_{a2} is connected to ground, while the bottom plates of C_{b1}, C_{b2}, and C_{b3} are connected to V_{EB2}. The voltage across C_{a2} is V_{EB1}, while the voltage across C_{b1}, C_{b2}, and C_{b3} is ΔV_{BE}. Nodes *3* and *4* are charged to V_{EB1}. In phase φ_1, C_{a1} and C_{a2} are connected together. As C_{a1} was charged to ground and C_{a2} was charged to V_{EB1} in phase φ_2, the voltage at node *3* in phase φ_1 is $V_{EB1}C_{a1}/(C_{a1}+C_{a2})$ (Fig. 5.4.2). Further, C_{b1}, C_{b2}, and C_{b3} are connected in series in phase φ_1 to generate $3\Delta V_{BE}$. The voltage at node *4* drives C_{REF} to a voltage $V_{REF}=3\Delta V_{BE}+V_{EB1}*C_{a1}/(C_{a1}+C_{a2})$. The capacitor values are selected to set a temperature independent V_{REF} accounting for bottom plate parasitics. The load capacitors for V_{EB} generation and the SCN circuit use NMOS capacitors, and the bandgap output and the ΔV_{BE} tripler circuit use MIM capacitors to reduce bottom plate parasitics. Further, C_{a1} has 4b trimming to control process drift.

Figure 5.4.3 shows the clock generation and switching control circuit for the BGR, which must produce dual phase clocks at a voltage over V_{EB} from a lower V_{in}. A PTAT current source with high power supply rejection gives a current controlled ring oscillator clock (CLK) of approximately 30kHz at a V_{in} of 0.5V at approximately 2nW. A clock doubler circuit doubles the swing of the output clocks to enable the SCN switches to pass a V_{EB} voltage level. The output frequency of CLK is $3I_0/C_0V_{in}$, which is inversely proportional to V_{in} (Fig. 5.4.3), with I_0 being almost constant with V_{in}. Since the BGR power consumption increases with V_{in}, the decreasing frequency of the clock source with increasing V_{in} keeps the power consumption low. An increase of V_{in} from 0.5V to 1.5V decreases the period of CLK and the power of the BGR by 2×. CLK is used to generate two non-overlapping clock phases, p_1 and p_2, that swing from 0 to V_{in}. Phases p_1 and p_2 are used in the clock doubler circuit to generate signals that swing from 0 to $2V_{in}$ (Fig. 5.4.3). The bottom plates of C_{d1} and C_{d2} are connected to the output of inverters driven by p_1 and p_2, and their top plates are driven by diode connected L_{VT} NMOS devices whose leakage will charge the top plate to V_{in} in the absence of switching. The bottom plate of C_{d1} and C_{d2} swing from 0 to V_{in} when switching, and the top plate swings from V_{in} to $2V_{in}$ (Fig. 5.4.3). Next, we convert these signals to full 0-to-$2V_{in}$ swing. When p_1 is high, X_2 is also high, so φ_2 is pulled down to ground. When p_1 is at 0, X_2 is at V_{in} and X_1 is at $2V_{in}$. The PMOS transistor will turn on and pass the X_1 level to φ_1, which swings from 0 to $2V_{in}$. Similarly φ_2 also swings from 0 to $2V_{in}$ with a non-overlapping phase (Fig. 5.4.3).

The proposed BGR targets an output voltage of 500mV. Figure 5.4.4 shows the measured V_{REF} across process, temperature (0°C to 80°C), and V_{in} (0.5V to 1.5V). The BGR should operate to below 0.4V V_{in}, but limitations of unrelated circuits on the chip prevent measurement below 0.5V. The measured output voltage from 0°C to 80°C for 6 chips varies from 492mV to 504mV in the absence of trimming (Fig. 5.4.4). After applying one time trimming by changing C_{a1} (Fig. 5.4.2), the output voltage changes from 499.5mV to 504mV. The temperature stability of the BGR circuit varies from 75ppm/°C to 125ppm/°C across 6 chips. The untrimmed output of the BGR achieves a 3σ variation of approximately 2% across process at 0.5V V_{in} and 20°C (Fig. 5.4.4), which can be reduced by trimming C_{a1}. Figure 5.4.4 shows that the output varies by approximately 2% for a V_{in} variation from 0.5V to 1.5V for 6 chips, showing a PSR of -40dB at DC. Cascading two bandgap references, as shown in Fig. 5.4.5, can further reduce the PSR of the BGR. A voltage follower stage buffers the output of the first stage BGR and drives a 2nd stage BGR circuit. The lower current consumption of the BGR circuit enables the operation from a low quiescent current voltage follower stage. The output of the 2nd stage BGR, $V_{REF,PS}$ varies by 0.5% for the variation of V_{in} from 0.55V to 1.5V, showing a PSR of -52dB at DC.

Figure 5.4.5 also shows the BGR power consumption, which is 32nW at 0.5V V_{in} and 27°C. The current source and ring oscillator consume 10.5nW, so the BGR power consumption could be reduced to 21.5nW with an external clock, if already available in a system. The BGR circuit should function to 0.4V, where it consumes 19.2nW. The power consumption of the cascaded BGR circuit to generate $V_{REF,PS}$ is 71nW, or 52nW with an external clock source. Figure 5.4.5 shows the settling time of the BGR circuit at different V_{in} to be below 5ms. The ripple on V_{REF} is 50µV at a V_{in} of 0.5V.

Figure 5.4.6 compares this work with previously reported state-of-the-art low power BGR circuits. The BGR in this work operates at 0.5V, over 1.4× lower than in [2], and the design supports even lower V_{in}. The BGR consumes 32nW at 0.5V V_{in}, which is over 1.6× lower than [2]. Further, [3] uses a switched-capacitor BGR circuit to reduce area and achieves lower power by duty cycling, which results in a ripple of 20mV. The ripple of our BGR is due to clock feedthrough and is measured at 50µV at 0.5V V_{in}. The temperature stability of our BGR is 75ppm/°C from 0°C to 80°C. References [4] and [5] achieve higher temperature stability but consume 600× more power. The PSR of our circuit is –40dB or -52dB at DC in the two design options. Further, conventional lower voltage BGRs [1] require large resistors for low power, which increases area. Our BGR does not use resistors and has an area of 0.0264mm^2.

The proposed bandgap circuit is implemented in 0.13µm CMOS (Fig. 5.4.7). It improves the power consumption by 1.6× and minimum operating voltage by 1.4× compared to similar work.

References:

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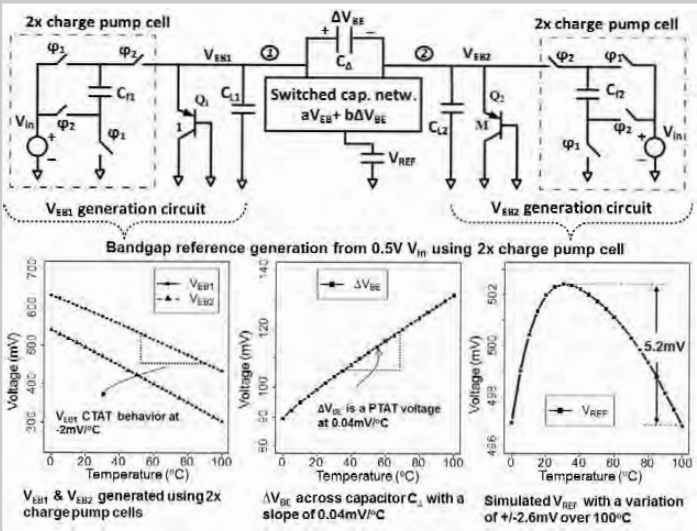


Figure 5.4.1: Circuit diagram and V_{EB}, ΔV_{BE}, and V_{REF} simulations for the bandgap reference circuit.

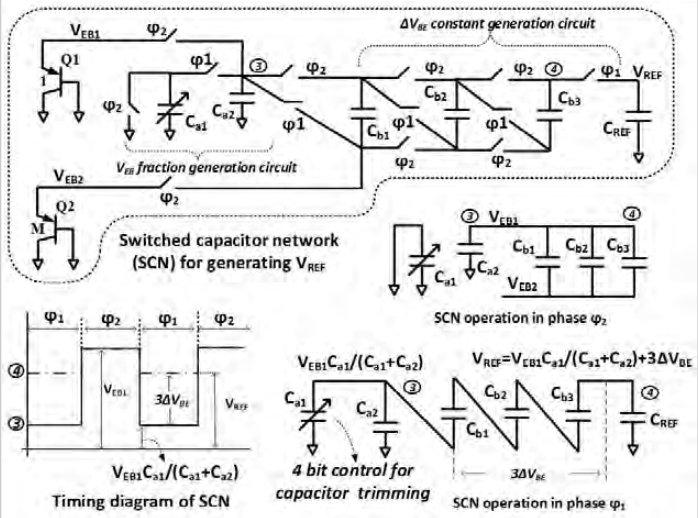


Figure 5.4.2: Switched-capacitor network circuit used by the BGR to generate a ratio and sum to obtain V_{REF}.

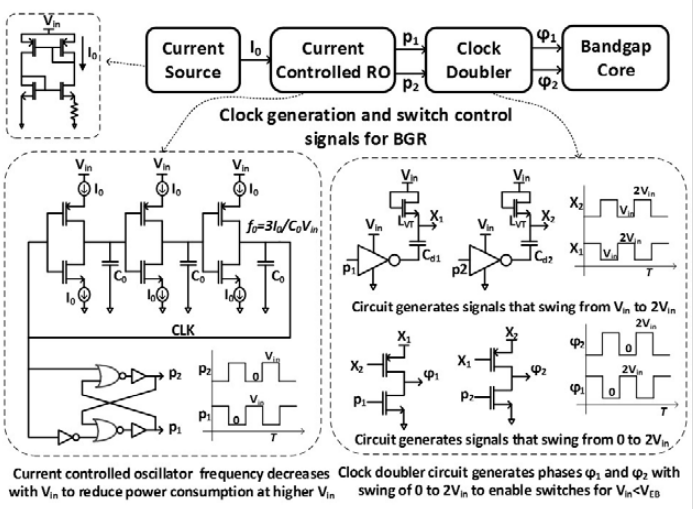


Figure 5.4.3: Clock generation and switch control signals used to enable switching for the BGR core circuit.

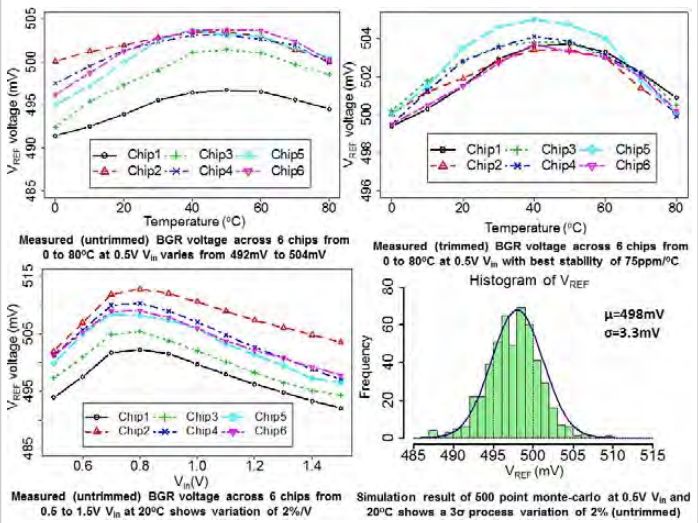


Figure 5.4.4: Measurement of the variation of BGR circuit across temperature, V_{in}, and process.

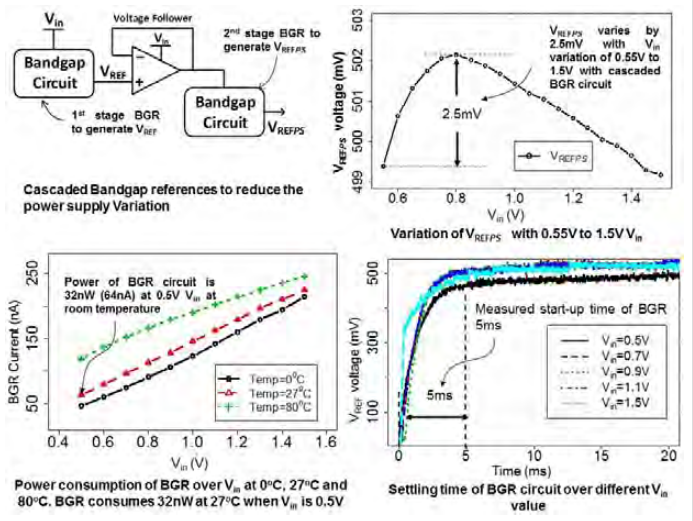
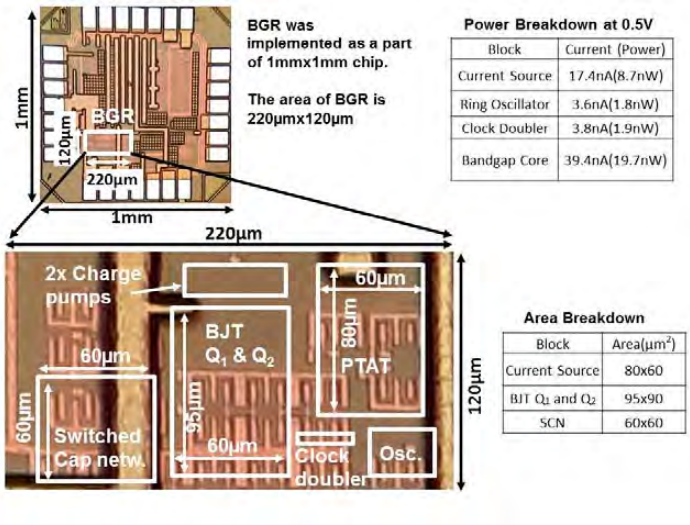


Figure 5.4.5: Variation of the BGR voltage, power consumption and settling time with V_{in}.

	[1]	[2]	[3]	[4]	[5]	[6]	This work
Process Technology	0.4μm	0.18μm	0.13μm	0.5μm (BICMOS)	0.16μm	0.35μm	0.13μm
Power Consumption	1.85μW	52.5nW	170nW	20μW	99μW	300nW	32nW
Minimum V_{in}(V)	0.84	0.7	0.75	1	1.62	1.4	0.5
Temp. variation (ppm/°C)	119	114	40	11	5	7	75
Untrimmed accuracy (3σ) %	5.8	4.8	3	1.1	1.5	21	2
PSR (dB)	-57@DC	-56@100 Hz	-93@DC	-86@DC	-74@DC	-45@100 Hz	-40 @ DC/ -52 @ DC*
Ripple	NA	NA	20mV	NA	NA	NA	50μV
Always on BGR	✓	✓	×	✓	✓	✓	✓
Area (mm²)	0.1	0.0246	0.07	0.4	0.12	0.05	0.0264

*Power Consumption at -52dB PSR is 71nW

Figure 5.4.6: Comparison of BGR metrics with other low power, low V_{in} designs.



Power Breakdown at 0.5V

Block	Current (Power)
Current Source	17.4nA(8.7nW)
Ring Oscillator	3.6nA(1.8nW)
Clock Doubler	3.8nA(1.9nW)
Bandgap Core	39.4nA(19.7nW)

Area Breakdown

Block	Area(μm^2)
Current Source	80x60
BJT Q_1 and Q_2	95x90
SCN	60x60

Figure 5.4.7: Die micrograph of the bandgap reference circuit.

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