5.3 A 2-Channel -83.2dB Crosstalk 0.061mm² CCIA with an Orthogonal Frequency Chopping Technique

Yi-Lin Tsai, Feng-Wen Lee, Tzu-Ying Chen, Tsung-Hsien Lin

National Taiwan University, Taipei, Taiwan

Area-efficient low-noise instrumentation amplifiers (IAs) are required in various multi-channel sensing and monitoring applications. These IAs must be designed to achieve low noise and low power, good noise efficiency factor (NEF), good gain matching and low crosstalk among multiple channels [1]. For a continuous sensor array application, each sensor unit is conventionally connected to an individual amplifier for analog signal processing. This configuration consumes large chip area and high power. Furthermore, the quality of gain matching among channels is limited due to the independence of each channel. In [2-3], several multi-channel schemes addressing some of these difficulties are reported. This paper demonstrates a prototype capacitively-coupled IA (CCIA) that adopts an orthogonal frequency chopping (OFC) technique to realize a continuous two-channel CCIA with only one active amplifier, thus saving chip area and power. The whole two-channel CCIA, realized in 0.35μm CMOS, occupies an active area of 0.061mm² (area per channel is 0.0305mm²). This 2-channel IA draws 27μA from a 3V supply. It achieves a low input-referred noise of 26nV/√Hz, reasonable NEF of 3.74, and good gain matching with mismatch of less than 0.55%. The average crosstalk between two channels is -83.2dB, which is about 10dB better than those reported in designs of similar framework [2-3].

Figure 5.3.1 shows the block diagram of the reported 2-channel CCIA and illustrates the frequency domain operation. While this operation concept can be in principle extended to an *n*-channel design, a 2-channel prototype is demonstrated in this work. In this circuit (Fig. 5.3.1), two chopping frequencies, f_1 and f_2, are applied to modulate and demodulate the 2 input signals, V_1 and V_2, respectively, while sharing a single CCIA. It can be observed that if f_1 and f_2 are orthogonal, the 2 output signals, V_{01} and V_{02}, contain only the corresponding amplified signals with respect to inputs V_1 and V_2. The crosstalk signals from the adjacent channel are shifted out of baseband and can be eliminated by subsequent analog signal processing circuits, such as a lowpass filter. To ensure orthogonality in this work, $f_1=f_{chop}$ and $f_2=2f_{chop}$. If f_1 and f_2 are both 50% duty-cycled square-wave signals, the first chopper modulates V_1 to odd harmonics of f_{chop}, appearing at f_{chop}, $3f_{chop}$, $5f_{chop}$, etc. Meanwhile, V_2 is modulated to odd harmonics of $2f_{chop}$, appearing at $2f_{chop}$, $6f_{chop}$, $10f_{chop}$, etc. Both modulated signals traveling through the CCIA are demodulated back to baseband and appear only at the respective output terminals. In an *n*-channel CCIA adopting the OFC technique, the chopping frequencies can be selected as $f_i=(2^{i-1})f_{chop}$, i=1 to *n* (i.e., $f_1=f_{chop}$, $f_2=2f_{chop}$, $f_3=4f_{chop}$, $f_4=8f_{chop}$, for *n*=4). As the number of shared channels, *n*, increases, the area reduction due to the reduced number of opamps (*n*-1) also increases. On the other hand, the design requirement of the shared opamp is more stringent as the opamp must accommodate a higher frequency. The optimum choice of *n* depends on which factor (chip area or power) is the primary design consideration in a given system.

Figure 5.3.2 shows the schematic of the 2-channel CCIA. It is composed of a shared opamp, two chopper pairs, and T-bridge capacitors. In the shared opamp, low noise and low power are the main design considerations. The PMOS (M_1, M_2) and NMOS (M_3, M_4) pairs, operated in a current-reused topology, are adopted as the input stage to boost the input transconductance. The circuit is biased at the sub-threshold region for achieving a high g_m/I_D value. The transistor aspect ratio (W/L) is designed to be large to suppress flicker noise and lower the flicker corner frequency. The chopping frequencies, f_1 and f_2, are chosen to be 10kHz and 20kHz, respectively. In the CCIA, the feedback resistor is often quite large so as to create a very low high-pass corner frequency. Pseudo resistors, consisting of two PMOS transistors operated in the sub-threshold region, are used as the feedback resistor to provide ultra-large area-efficient resistance. In this work, the gain of CCIA is designed to be 40dB, which is determined by the capacitance ratio of the input and feedback capacitors. To lower the chip area, the input capacitors must be aggressively minimized; however, the proportionally reduced feedback capacitors result in worse matching, which in turn degrades gain accuracy as well as gain matching. To address this issue, the T-bridge topology is adopted to synthesize the feedback capacitance. In this design, a minimum capacitance of 100fF is chosen for matching considerations and reduced sensitivity to other parasitic capacitances. With $C_1=C_2=100fF$, $C_3=800fF$, and $C_{in}=1pF$, a 40dB gain with sufficient accuracy and matching quality is ensured. In an *n*-channel CCIA, each input path is chopped at a different frequency, which leads to a different input impedance as seen by each sensor. By lowering the input capacitance, the input impedance can be boosted sufficiently to offer design margin against different chopping frequencies at each signal path.

The 2-channel CCIA employing the OFC scheme is fabricated in 0.35μm CMOS process technology. The total active area is 0.061mm²; the effective area per channel is 0.0305mm². Operated from a 3V supply, this 2-channel CCIA draws 27μA with each channel consuming an equivalent current of 13.5μA. To verify the effectiveness of the OFC technique, the crosstalk between channels is measured by applying a sinusoidal input signal to channel 1 of the CCIA while the input of channel 2 is kept at the common mode. 10 samples were measured with the input frequency varying from 100Hz to 1kHz. The measured crosstalk (upper left of Fig. 5.3.3) ranges from -79dB to -89dB, with an average of -83.2dB. The upper-right plot of Fig. 5.3.3 shows the measured outputs (overlay plot) when 2 signals at 500Hz and 550Hz are applied to channel 1 and channel 2, respectively. When monitoring channel 2 alone (lower-left of Fig. 5.3.3), the small signal leakage from channel 1 at 500Hz is observed. Comparing these two plots indicates that the crosstalk from channel 1 is -83dB. Similarly, the signal leaking from channel 2 to channel 1 (lower-right of Fig. 5.3.3) is at -92dB, while the signal magnitude is at -11dB; the crosstalk is around -81dB.

The total harmonic distortion (THD) of the CCIA at an input magnitude of $4mV_{pp}$ is dominated by the 3rd harmonic, which is at -67.2dB, as shown in Fig. 5.3.4. Tones at 60Hz with harmonics at 180Hz and 300Hz result from supply line noise. The output noise density, measured by an Agilent 35670A dynamic signal analyzer, is 2.6μV/√Hz (Fig. 5.3.5). With a CCIA gain of 40dB, the input-referred noise density is 26 nV/√Hz. The NEF of the proposed IA is calculated to be 3.74. The measured gain mismatch between channels for a sinusoidal input signal is around 0.55%. CMRR is higher than 110dB and PSRR is better than 103dB up to 1kHz. The experimental results are summarized and compared with state-of-the-art IAs in Fig. 5.3.6. The chip micrograph is shown in Fig. 5.3.7.

Acknowledgement:
The authors thank Y.-Y. Lin and Y.-F. Kuo for valuable discussion, and CIC, Taiwan for chip fabrication. This work is supported by MOST, Taiwan.

References:
[1] Q. Fan, et al., "A 1.8μW 60nV/√Hz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes," *IEEE J. Solid-State Cicruits*, vol. 46, no. 7, pp. 1534-1543, July 2011.
[2] F. Sebastiano, et al., "A 0.07mm² 2-Channel Instrumentation Amplifier with 0.1% Gain Matching in 0.16μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 294-295, Feb. 2014.
[3] B. Johnson, A. Molnar, "An Orthogonal Current-Reuse Amplifier for Multi-Channel Sensing," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp.1487-1496, June 2013.
[4] I. Akita, M. Ishida, "A 0.06mm² 14nV/√Hz Chopper Instrumentation Amplifier with Automatic Differential-Pair Matching," *ISSCC Dig. Tech. Papers*, pp. 178-179, Feb. 2013.
[5] F. Michel, M. Steyaert, "On-chip Gain Reconfigurable 1.2V 24μW Chopping Instrumentation Amplifier with Automatic Resistor Matching in 0.13μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 372-373, Feb. 2012.

 978-1-4799-6224-2/15/$31.00

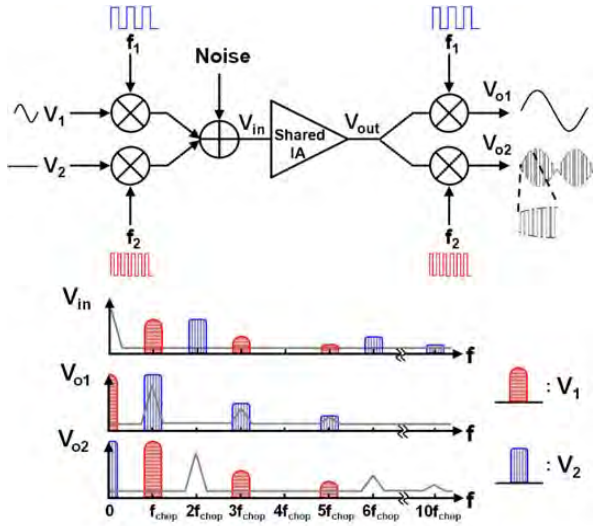

Figure 5.3.1: Overall architecture and the concept of the orthogonal frequency chopping technique.

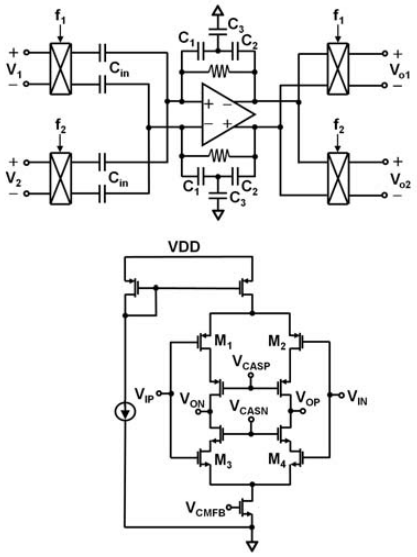

Figure 5.3.2: CCIA with the operational amplifier.

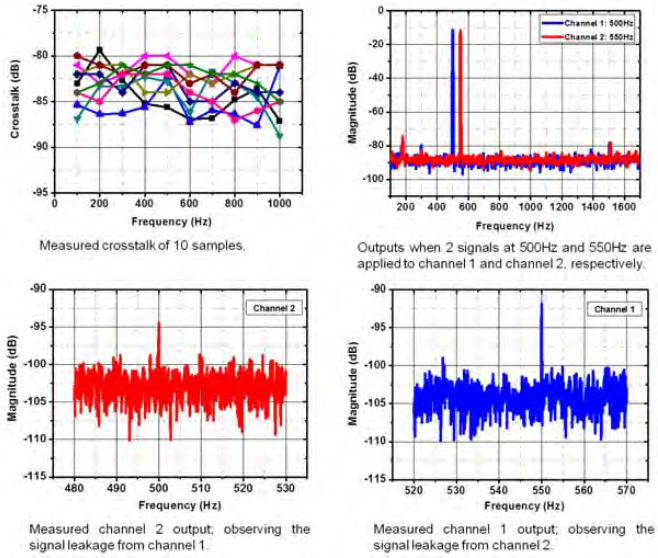

Figure 5.3.3: Crosstalk performance between two channels.

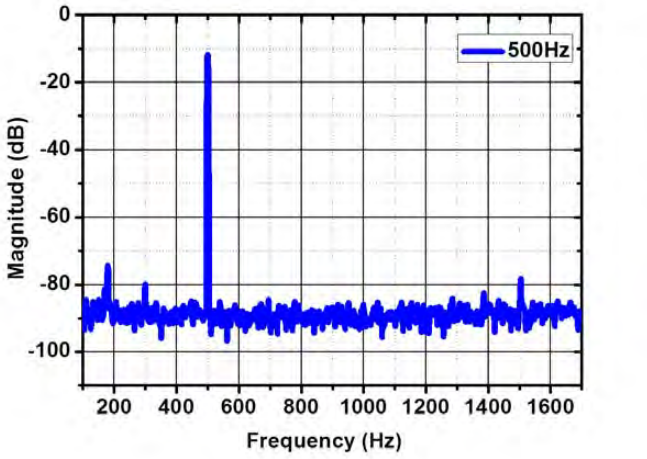

Figure 5.3.4: Measured output harmonic distortion (input magnitude=4mVpp); THD is dominated by the 3rd harmonic tone (-67.2dB). Tones at 180Hz and 300Hz are due to supply line noise.

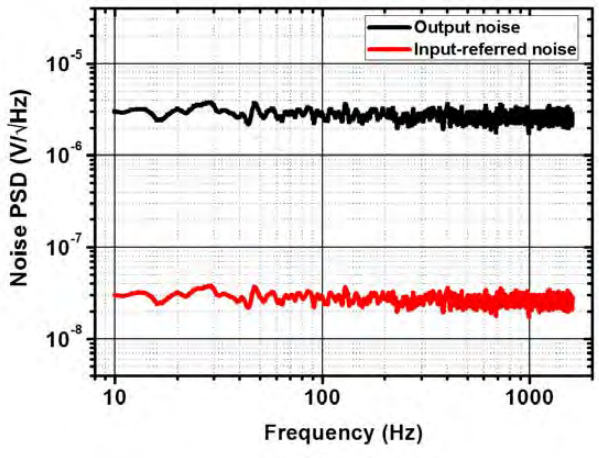

Figure 5.3.5: Measured output noise PSD and input-referred noise PSD.

	This work	ISSCC'14 [2]	JSSC'13 [3]	ISSCC'13 [4]	ISSCC'12 [5]
Technology (μm)	0.35	0.16	0.13	0.18	0.13
Chopper (Y/N)	Y	Y	N	Y	Y
f_1 (kHz)	10	200 (100*)	-	500	25
f_2 (kHz)	20	-	-	-	-
Supply Voltage (V)	3	1.8	1.5	1.5	1.2
Current (μA)	13.5	320	2.6	194	31
Input Noise PSD (nV/√Hz)	26	18.7	26.2**	13.5	40
CMRR (dB)	110	>99	78	102	116
PSRR (dB)	103	>102	80	101	108
Crosstalk (dB)	-83.2	-73	-50	-	-
Gain Matching (%)	0.55	0.1	7	-	±0.7
NEF	3.74	12.9	1.64	7.2	7.5
Number of Samples	10	40	N/A	12	8
Area (mm^2) (Per channel)	0.0305	0.035	0.03125	0.06	0.465

*Additional 100kHz clock for DEM
**Equivalent number is calculated from NEF in [3]

Figure 5.3.6: Performance summary and comparison table.

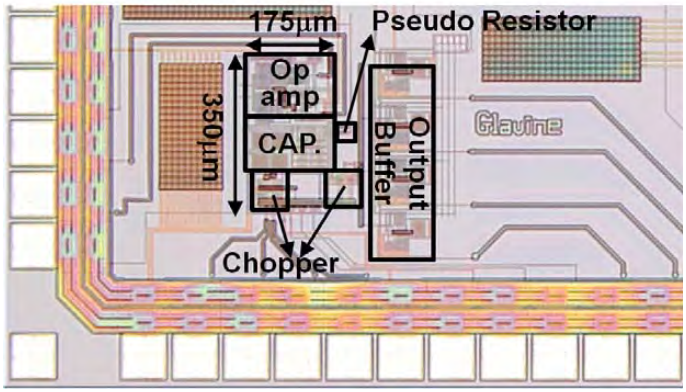

Figure 5.3.7: Chip micrograph.

978-1-4799-6224-2/15/$31.00