5.2 A 110dB SNR ADC with ±30V Input Common-Mode Range and 8μV Offset for Current Sensing Applications

Long Xu[1], Burak Gönen[1], Qinwen Fan[2], Johan H. Huijsing[1], Kofi A. A. Makinwa[1]

[1]Delft University of Technology, Delft, The Netherlands,
[2]Maxim Integrated Products, Delft, The Netherlands

This paper presents a high-resolution 110dB SNR ΔΣ ADC that achieves a ±30V input common-mode voltage range (CMVR) while powered from a single 5V supply. This beyond-the-rails capability is obtained by employing a capacitively coupled high-voltage (HV) chopper at the input of a switched-capacitor (SC) ΔΣ ADC. Furthermore, the use of correlated double sampling and system-level chopping results in a maximum offset of 8μV over the full CMVR. In contrast to a recent HV ADC [1], the ADC exhibits 30dB more resolution, while its CMVR extends below the negative rail.

The ADC is intended for current monitoring applications, in which a small voltage drop across a shunt resistor must be digitized. In battery monitoring applications, or when inductive loads are involved, the differential voltage across the shunt will often be accompanied by beyond-the-rails common-mode (CM) voltages. Conventionally, current monitoring systems consist of a precision current sensing amplifier (CSA) with a wide CMVR, whose output is then digitized by an ADC [2]. The CSA thus isolates the ADC from large CM voltages, while its gain relaxes the ADC noise requirements. Since the presented ADC itself has beyond-the-rails CM capability together with high resolution, low offset and high gain accuracy, it obviates the need for the CSA, thus reducing the power consumption and the silicon area of the resulting current monitoring system.

Figure 5.2.1 shows the block diagram of the ADC. It consists of a single-loop single-bit 3rd-order SC ΔΣ ADC with a feed-forward architecture based on three OTAs and a SC summing network. An inner set of HV choppers, CH_{in}, together with switches Φ1 and Φ2, implement a correlated double sampling (CDS) scheme that mitigates the effect of offset and 1/*f* noise of the 1st OTA. Further offset reduction is obtained with the help of an outer set of HV choppers, CH_{sys}, which, together with a digital chopper at the output of the modulator, implement a system-level chopping scheme. During Φ1, the input signal, V_{in}, and the OTA offset are sampled on the 5pF input capacitors, C_s. During Φ2, the HV chopper, CH_{in}, reverses the input and thus transfers a charge packet proportional to $2 \bullet C_s \bullet V_{in}$ to the integration capacitors, C_{int}. This cross-coupled sampling scheme [3] ensures that the only components exposed to the input CM voltage are the capacitors C_s and two capacitively coupled HV choppers. The input capacitors are implemented as HV fringe capacitors with a breakdown voltage of 80V. The feedback capacitors are also implemented with the same type of capacitors, to ensure good matching and hence, good gain accuracy.

Figure 5.2.2 shows the schematic of the capacitively-coupled HV chopper, which consists of 4 sampling switches MN_{1-4}, one dynamic latch $MN_{5,6}$, three coupling capacitors C_{1-3} and a minimum selector MN_{S1-2}. All the transistors are 5V NMOS devices located in an isolated HV N-Epi pocket (Fig. 5.2.2). The N-Epi pocket is capable of floating up to 65V with regard to the grounded P-Substrate, while the local P-wells can float down to -60V with respect to the N-Epi pocket. Potential latch-up issues associated with the parasitic NPNP structure of the NMOS transistors are circumvented by two measures: 1) The minimum selector prevents the upper NP-diode from conducting, and 2) An HV clamping diode between the positive supply and the floating N-Epi prevents the N-Epi pocket from dropping below the P-Substrate, which means that the lower NP-diode cannot turn on. Protection devices MN_{7-9} and D_{1-6} restrict the maximum voltage drop across MN_{1-4} to less than 5V, even during fast CM transients. In this way, the HV chopper switches can withstand ±60V input CMVR. In the end, the ADC input CMVR is limited to ±30V by the ESD diodes at the input terminals.

In a previous floating HV chopper [4], the sources of the 4 switches were connected to their P-wells. As a result, the parasitic drain/P-well diodes, Dp_{1-4}, limited the input differential voltage range (DVR) of the chopper to several hundred millivolts. To extend the DVR, a minimum selector, MN_{S1-2}, is connected to the chopper input terminals. The circuit ensures that the P-wells of the switches are connected to the input terminal with the lowest input voltage, V_{min}, thus ensuring that parasitic diodes Dp_{1-4} are not forward biased.

Each HV chopper is controlled by non-overlapping clock signals Clkp and Clkn, generated by standard 5V logic, which are capacitively coupled to the gates of transistors MN_{1-4} via capacitors C_{1-3}. In [4], the initial gate voltages of MN_{1-4} are defined by connecting the sources of the latch MN_{5-6} (node A) to one of the input terminals, say V_{inp}. If V_{inp} is higher than V_{inn}, and the differential switch input voltages are larger than the threshold voltages, the switches $MN_{2,4}$ connected to the terminal V_{inn} will never turn off. To avoid this, node A is connected to the output of a minimum selector so that the clock signals are always superimposed on V_{min} (the lower of V_{inp} and V_{inn}). Due to the cross-coupled sampling scheme, the 4 switches of the HV chopper can share one set of coupling capacitors. Compared to other HV switches [5], this capacitively coupled HV chopper is 3× smaller, occupying only 0.012mm^2.

Since the coupled clock signals are superimposed on $V_{min,}$ their amplitude determines the maximum DVR of the chopper switches. This is because the switches can only be turned on if the amplitude of the differential input signal is less than their overdrive voltage. However, it should be noted that the coupled signals at the gates of the switches are slightly attenuated by the parasitic capacitors at nodes B, C. As a result, with 0-to-5V clock signals, the measured linear differential input range of the chopper is about $4.4V_{p\text{-}p}$.

The first integrator is implemented around a folded-cascode gain-boosting OTA, which achieves 120dB DC gain and draws 40μA. The second and third integrators are scaled down to improve power efficiency. They are built around single-stage folded-cascode OTAs, each of them has a gain of 90dB and draws 5μA. The comparator is composed of a pre-amplifier and a dynamic latch. For flexibility, the decimation is performed by an off-chip 512-tap sinc^3 filter.

The ΔΣ modulator is realized in an HV 0.18μm CMOS process (Fig. 5.2.7). It has an active area of 0.8mm^2 and draws 101μA from a 5V supply. The sampling frequency is 150kHz and the signal bandwidth is 100Hz. Figure 5.2.3 gives the 2^{22}-point FFT output spectrum for a -6.2dB input signal (relative to the 2.8V reference of the ADC) that is superimposed on a 25V CM voltage. Figure 5.2.4 shows the measured SNR/SNDR versus input amplitude. As expected, the modulator exhibits a soft clipping characteristic as the HV choppers gradually run out of overdrive. The peak SNR, SNDR and SFDR are 110.1dB, 100.6dB and 100.8dB respectively. The peak SNDR varies by 0.5dB over the ±30V CMVR, demonstrating the excellent linearity of the HV chopper over the full CMVR. Figure 5.2.5 depicts the low frequency characteristics of the ADC obtained from 15 samples. Its offset is less than 250μV with CDS alone, which improves to 8μV after system-level chopping (at 0.5Hz) and, in both cases, changes by less than ±2μV over the full CMVR. The ADC gain accuracy is better than 0.6%, while its DC CMRR is always greater than 140dB. Although the CMRR rolls off with frequency, it is still greater than 110dB and 72dB at 0.5Hz and 50Hz, respectively. The ADC performance is summarized in Fig. 5.2.6. Compared with [1], the proposed ADC extends the input CM voltage below the negative rail, and achieves a 30dB higher SNR. Furthermore, compared to [4], the improved HV chopper exhibits a 15× larger DVR, while maintaining the same input CMVR.

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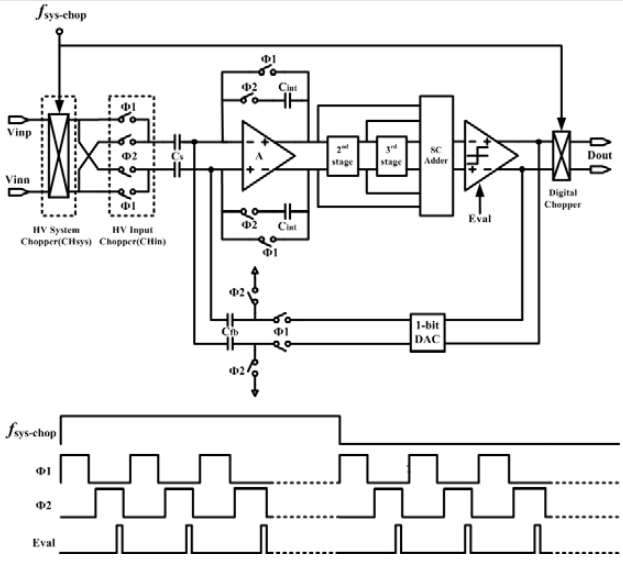

Figure 5.2.1: Block and timing diagrams of the 3rd-order ΔΣ ADC.

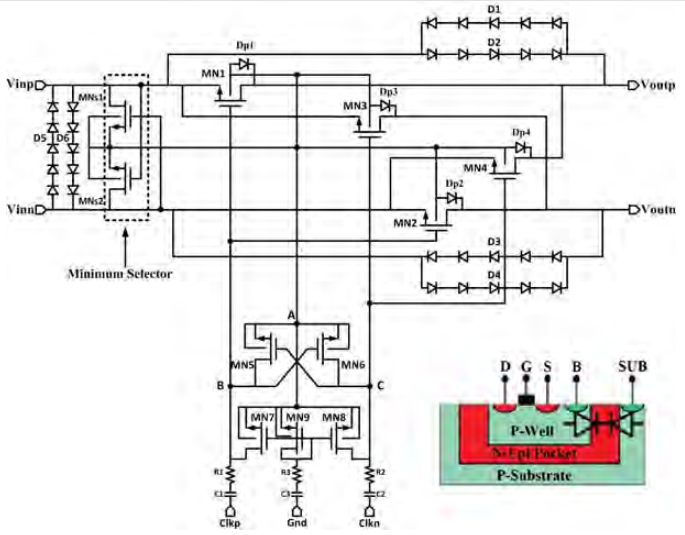

Figure 5.2.2: Schematic of the HV input chopper and a cross-section of the NMOS devices.

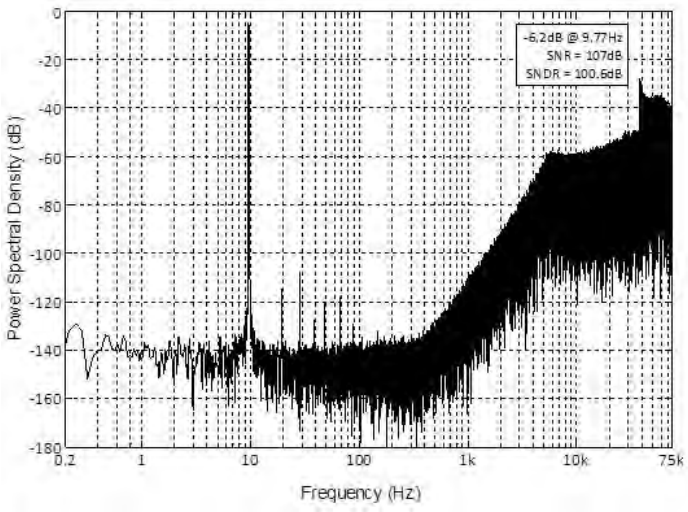

Figure 5.2.3: Measured 2^{22}-point FFT of the ΔΣ modulator output (V_{CM}=25V).

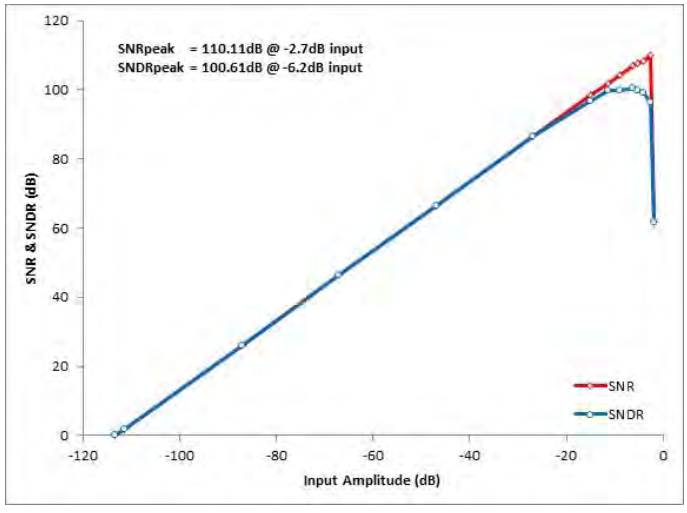

Figure 5.2.4: SNR and SNDR versus input amplitude.

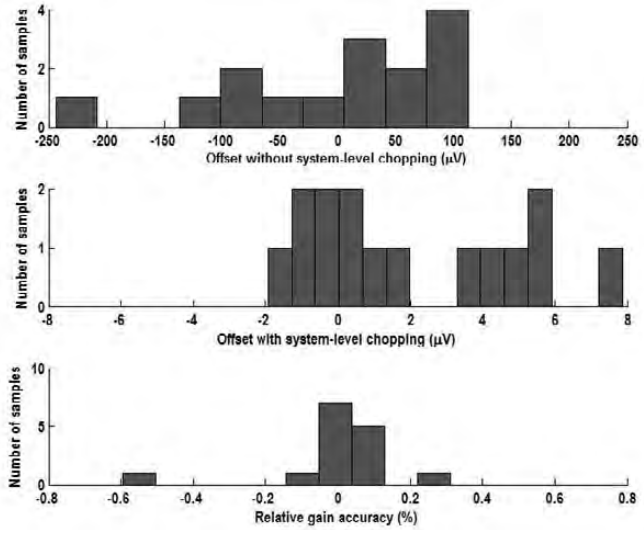

Figure 5.2.5: Histograms (15 samples) of the measured offset (with and without system-level chopping) and the relative gain accuracy.

	This work	[1]	[2]
Supply voltage	5V	3.3V	2.7V-5.5V
Input CM range	±30V	0-50V	0-60V
Input DM range	$4.4V_{p-p}$	$50V_{p-p}$	$440mV_{p-p}$
SNR	110.1dB	81dB	73.98dB
SNDR	100.6dB	80.6dB	--
SFDR	100.8dB	97.8dB	--
BW	100Hz	125kHz	500Hz
Offset	8μV	--	500μV
CMRR (@DC)	140dB	--	120dB
PSRR (@DC)	80dB	--	77dB
Gain accuracy	0.6%	--	--
Chip area	0.8mm²	0.98 mm²	--
Power	505μW	4.29mW	4.32mW
FOM*	163dB	155.6dB	124.6dB

* $FOM = SNR + 10\log(\frac{BW}{P})$

Figure 5.2.6: Performance summary and comparison table.

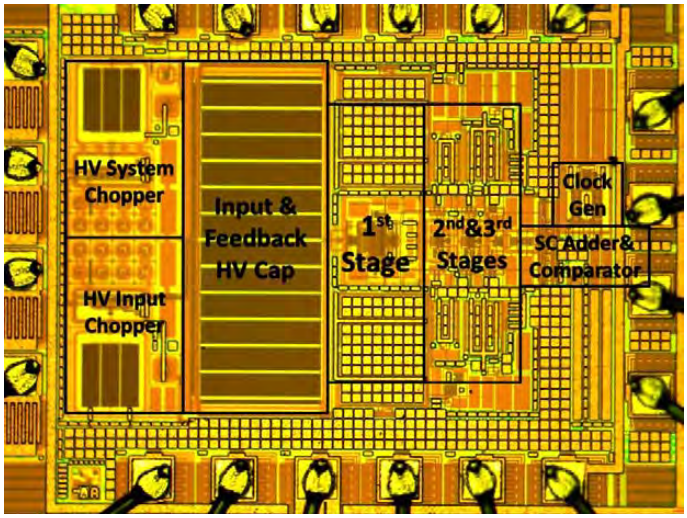

Figure 5.2.7: Chip micrograph.

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