5.10 A 4.7MHz 53μW Fully Differential CMOS Reference Clock Oscillator with –22dB Worst-Case PSNR for Miniaturized SoCs

Junghyup Lee[1], Pyoungwon Park[1], SeongHwan Cho[2], Minkyu Je[3]

[1]Institute of Microelectronics, Singapore, Singapore,
[2]KAIST, Daejeon, Korea,
[3]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea

Low-power CMOS reference clock oscillators have been widely used in miniaturized SoCs for emerging microsystems such as implantable biomedical devices and smart sensors [1-3]. In such SoCs, as the supply voltage shrinks and the level of analog and digital circuit integration increases to meet rigorous power and area constraints, the noise from other blocks (especially digital blocks) couples through supply and ground lines and poses a serious threat to the performance of CMOS reference clock oscillators.

Although relaxation oscillators can provide high frequency stability as well as low noise [1-3], they have poor tolerance to supply and ground noise due to supply-sensitive building blocks such as reference voltage generators and single-ended comparators. One way of making them immune to the supply noise is to regulate the supply using a bandgap voltage regulator [4]. However, the regulator consumes large power and area and, moreover, requires large external decoupling capacitors of several hundreds of nF to remove high frequency noise, because the supply noise rejection of the regulator starts to deteriorate from around tens of kHz. This approach is therefore not suitable for more area- and power-restricted applications. In this paper, a low-power CMOS reference clock oscillator with high supply and ground noise rejection is presented, which achieves a worst-case power supply noise rejection (PSNR) of –22 dB without any help of decoupling capacitors and bandgap regulators by employing: 1) A fully differential supply- and ground-regulating frequency-locked loop (FLL) architecture; 2) A differential period detector (PD) with a supply-insensitive period reference, and 3) A differential integrator generating a virtual 0V reference. In addition, to achieve higher frequency stability and lower noise, the oscillator uses a chopping technique.

In order for the CMOS oscillators to achieve high immunity against supply and ground noise, it is important to secure a supply-insensitive period (or frequency) reference based on a differential topology. Such requirements can be achieved through a simple differential RC circuit shown in Fig. 5.10.1. To investigate the circuit, transient results of a capacitor voltage, V_C, after switching off, observed with various supply voltages are shown together. It can be seen that the 0V-crossing time, T_{0V}, is independent of supply variation and determined solely by the resistance, R_{ref}, and the capacitance, C_{ref}. Therefore, the supply insensitivity can be naturally obtained by using T_{0V} as the period reference. Since the voltage, V_{PD}, sampled at t_{CLK} indicates the difference between T_{0V} and t_{CLK}, the circuit acts like a PD with a supply-insensitive period reference.

The proposed CMOS reference clock oscillator is shown in Fig. 5.10.2, which is composed of a differential PD, a differential integrator, a ring VCO and control logic. As the oscillator is based on a fully differential architecture, it is essentially robust to common-mode interruptions such as supply and ground noise. The key idea is to employ a FLL around the ring VCO so that its output frequency, f_{CLK}, is locked to the supply-insensitive T_{0V}. In order to compare f_{CLK} with T_{0V} and convert their difference into V_{PD}, the oscillator uses the differential PD based on the RC circuit shown in Fig. 5.10.1. In the differential integrator, V_{PD} is compared to 0V, which is inherently generated by a virtual short of the differential integrator, and the comparison result changes the VCO supply V_{REG}. The VCO then updates f_{CLK} and generates an additional 4 phases of the clock signal used to control the simple logic circuit. Note that the virtual 0V replaces a supply-sensitive physical reference voltage, and both the supply and ground of the VCO are regulated by the FLL, making the proposed oscillator robust against not only supply noise but also ground noise. Since the DC-offset and flicker noise of the integrator degrade the frequency stability against supply variation and the noise performance of the oscillator, a chopper stabilization is employed and a low-pass filter composed of R_{REG} and C_{REG} is added to filter out the noise from chopping switches.

The timing diagram and important waveforms of the proposed oscillator are shown in Fig. 5.10.3. The periodic operation consists of a reset phase, a period-detection phase and a charge-transfer phase. During the reset phase, *RST* is low and C_{ref} is discharged to $-V_{DD}$ (i.e., $V_C = -V_{DD}$). Next, in the period-detection phase, Q is low and C_{ref} is charged through the two R_{ref} resistors. Note that since Q is the output of the oscillator divided by two, V_C at the end of this phase represents the period difference between $1/f_{CLK}$ and T_{0V}. After that, when *SW* goes low, V_{PD} is updated by sampling V_C and compared with 0V through the differential integrator, which transfers the charge on C_{ref} to C_{INT} and changes V_{REG}. Due to the negative feedback formed by the FLL, V_{PD} at the charge-transfer phase reaches 0V and the output clock is finally locked at T_{0V}. Therefore, the output frequency after locking is expressed as $f_{CLK}=1/T_{0V}=1/2ln(2)R_{ref}C_{ref}$, which is independent of supply variation, as desired.

To investigate the supply-noise sensitivity of the proposed oscillator, transfer functions from V_{DD} to V_{REG} have been simulated and the results are shown in Fig. 5.10.4(a). In the oscillator, the PD is the only block sensitive to supply noise that has high-pass characteristics (V_{PD}/V_{DD}) due to the first-order noise shaping. The high-frequency noise from the PD is strongly suppressed by the FLL action, which shows low-pass characteristics (V_{REG}/V_{PD}). Consequently, the overall transfer function has a band-pass characteristic (V_{REG}/V_{DD}) with a peak gain at around 100kHz, which is the bandwidth of the FLL. In order to quantify the dynamic supply-noise sensitivity, the PSNR performance has been measured with a sinusoidal tone of $200mV_{PP}$, as shown in Fig. 5.10.4(b). The oscillator achieves a worst-case PSNR of –22dB at 100kHz without any internal or external decoupling capacitors. For comparison, the measurement results of the commercial silicon oscillator [4] are shown together. The proposed oscillator shows 31dB and 43dB lower PSNR compared to the commercial one, with and without a decoupling capacitor of 100nF, respectively.

The proposed oscillator is fabricated in a 0.18μm standard CMOS process and occupies an overall area of about $430\times200\mu m^2$, as shown in Fig. 5.10.7. Note that the oscillator includes neither internal decoupling capacitors nor bandgap regulators. The oscillator consumes 53μW from a 1.4V supply at the output frequency of 4.7MHz. Figure 5.10.5(a) shows the measured period jitter and accumulated jitter performances for the cases with and without chopping. The use of the chopping technique improves the long-term jitter by approximately a factor of two at the 10^{4th} cycles due to the flicker noise suppression, while degrading the period jitter by only 4ps. The inclining slope of $\sigma\sqrt{N}$ for the first 1000 cycles is clearly observed from the measured accumulated jitter. Figure 5.10.5(b) shows the measured frequency stability of the proposed oscillator. By removing the DC-offset of the integrator through the chopper stabilization so that the oscillator can be more precisely locked at T_{0V}, the frequency stability over supply variation is improved by more than 2.5 times and the oscillator achieves the frequency variation of less than ±0.2% for the supply change from 1.4 to 3.3V. For the temperature change from –40 to 125°C, the oscillation frequency varies by less than ±0.35%. The performance of the oscillator is summarized and compared with other state-of-the-art designs in Fig. 5.10.6. The proposed reference clock oscillator achieves a worst-case PSNR of –22dB without using decoupling capacitors or bandgap regulators, while providing the frequency stability comparable to that of other state-of-the-art works. Moreover, the lowest period jitter is achieved.

Acknowledgements:
This work is funded by SERC, A*STAR, Singapore, under the grant number 102 171 0163, as well as MEST and DGIST, Korea, under the grant number 14-BD-0404.

References:
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[4] Linear Technology, "LTC6930 Data Sheet." Accessed on Nov. 17, 2014, <http://cds.linear.com/docs/en/datasheet/6930fd.pdf>

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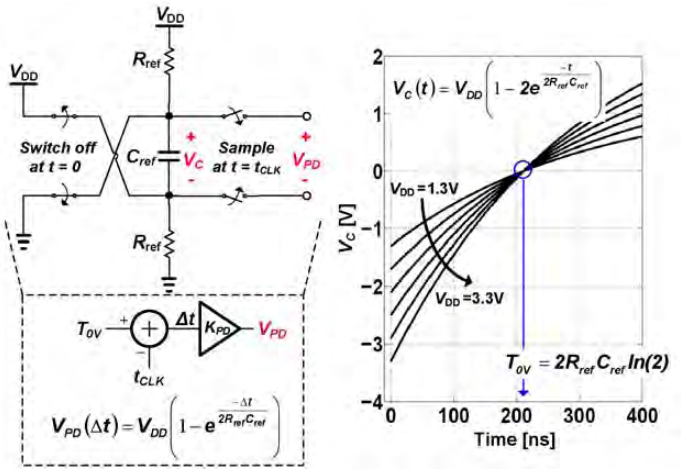

Figure 5.10.1: A differential RC circuit and its transient results under various supply voltages.

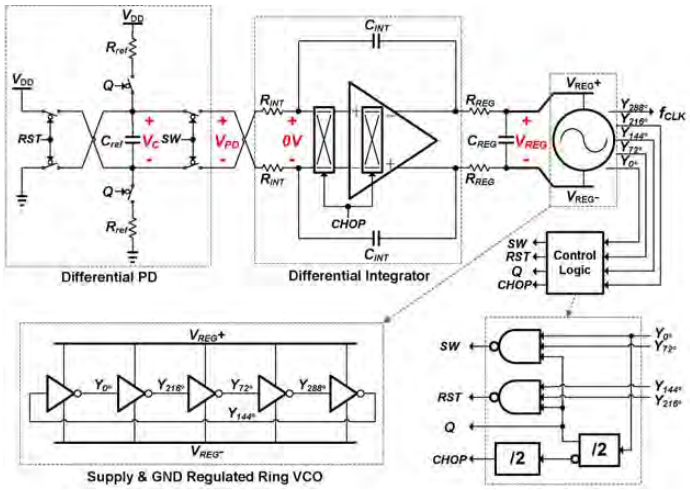

Figure 5.10.2: Structure of the proposed reference clock oscillator and schematics of the supply- and ground-regulated VCO and control logic circuit.

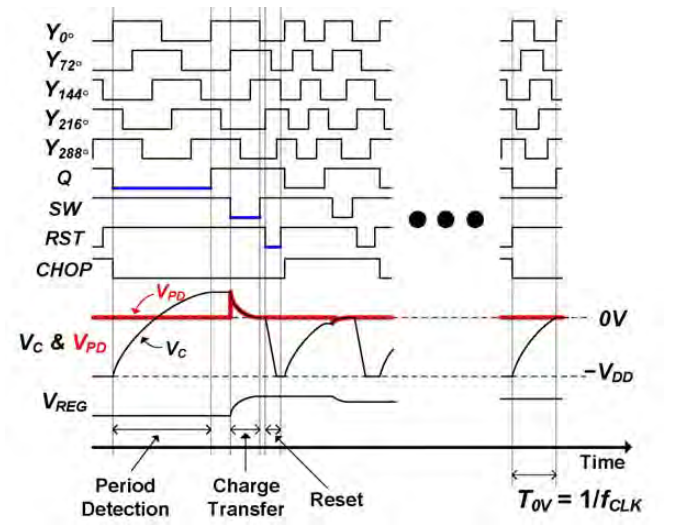

Figure 5.10.3: Timing diagram and waveforms of the reference clock oscillator.

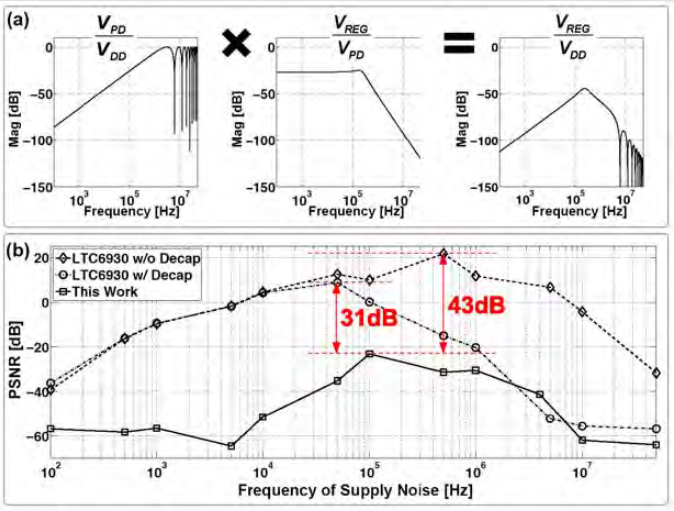

Figure 5.10.4: (a) Supply-noise transfer function of the oscillator. (b) Measured PSNR performance for the commercial [4] and proposed oscillators.

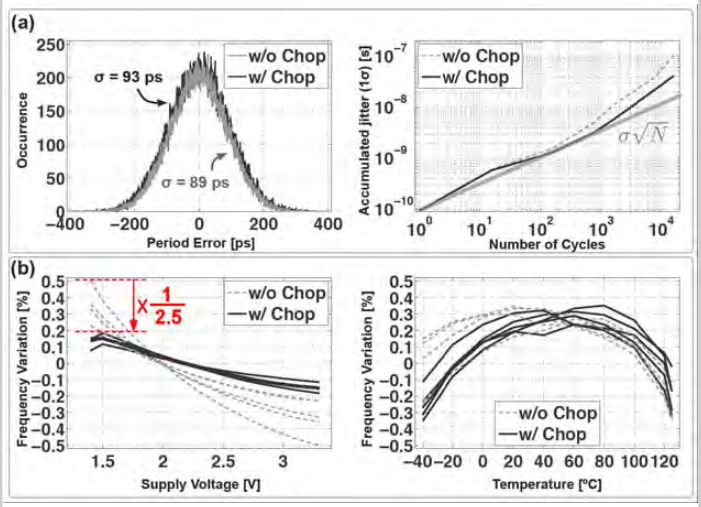

Figure 5.10.5: (a) Measured period jitter and accumulated jitter performances. (b) Frequency variations over supply and temperature measured for 5 samples.

Parameters	JSSC 2010 [1]	ISSCC 2009 [2]	ISSCC 2013 [3]	LTC6930 [4]	This Work
Technology [nm CMOS]	180	130	65	N/A	180
Decoupling Capacitor	N/A	N/A	N/A	Needed (100nF)	None
Supply Regulator	None	None	None	Needed	None
Frequency [MHz]	14	3.2	12.6	5	4.7
Area [mm²]	0.04 (Core)	0.073 (Core)	0.01 (Core)	N/A	0.086 (Overall)
Min. V_{DD} [V]	1.7	1.4	1.1	1.7	1.4
Power [µW]	45	38	98.4	340	53
Period RMS Jitter [%]	0.04	0.14	~0.07	0.11	0.04
Worst-Case PSNR [dB]	N/A	N/A	N/A	9[1]	-22
Freq. Variation [%] to V_{DD}	±0.16 @1.7 to 1.9V	±0.4 @1.4 to 1.6V	±0.07 @1.1 to 1.5V	±0.1 @1.7 to 3.7V	<±0.2 @1.4 to 3.3V
Freq. Variation [%] to Temp.	±0.19[2] @-40 to 125°C	±0.25 @20 to 60°C	±0.82 @0 to 80°C	<±0.6 @-40 to 125°C	<±0.35 @-40 to 125°C
Samples	1	1	1	Commercial Product	5

[1] With a decoupling capacitor of 100nF
[2] With a temperature compensation voltage

Figure 5.10.6: Performance summary and comparison.

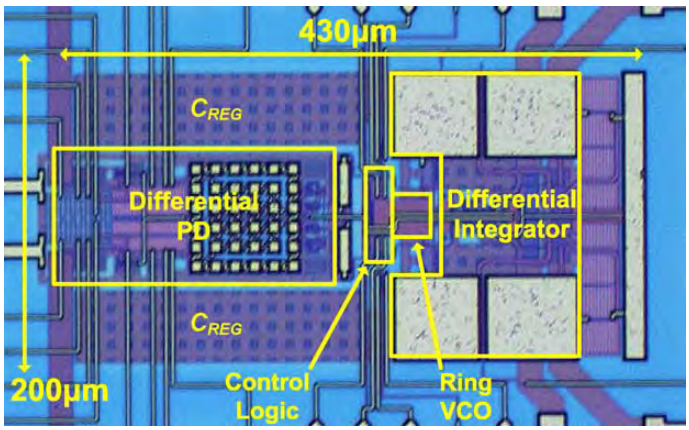

Figure 5.10.7: Die micrograph of the proposed reference clock oscillator.

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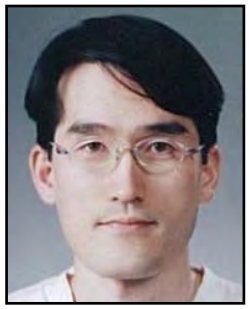
Session 6 Overview: *Image Sensors and Displays*

IMMD SUBCOMMITTEE

Session Chair: *Yusuke Oike, Sony, Atsugi, Japan*



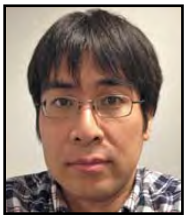
Session Co-Chair: *Young-Sun Na, LG Electronics, Seoul, Korea*

The session presents recent advancements in the field of image sensors and capacitive touch-sensing displays. The session starts with 3 papers on image sensors, including demonstrations of a back-illuminated stacked image sensor with highly parallel multi-sampling ADCs, the first 35mm-format image sensor for 8K video, and a low-power image sensor with a switchable "always-on" mode for mobile and wearable devices. The next 2 papers present a high-speed burst-mode image-acquisition system for scientific phenomena, and an event-driven motion detection system that uses in-pixel non-volatility analog memory for security applications. The latter part of the session presents recent achievements in the area of capacitive touch-sensing displays. This includes the first system where passive/active styluses and multi-fingers can simultaneously touch a 60-inch display. Another paper presents a system where touch is extended into the 3rd dimension for mobile applications. A 6b-resolution pen pressure sensor that uses a passive resonant stylus is introduced that can replace conventional costly Electro-Magnetic-Resonance-based touch systems.

6.1 A 1/1.7-inch 20Mpixel Back-Illuminated Stacked CMOS Image Sensor for New Imaging Applications **1:30 PM**

A. Suzuki, Sony, Atsugi, Japan

In Paper 6.1, Sony presents a 1/1.7-inch 20Mpixel back-illuminated stacked CMOS image sensor. The sensor achieves 1.3e-rms random noise with multiple sampling at 20Mpixel 30fps in addition to 16Mpixel 120fps readout with visually lossless data compression and two simultaneous output streams.



6.2 133Mpixel 60fps CMOS Image Sensor with 32-Column Shared High-Speed Column-Parallel SAR ADCs **2:00 PM**

R. Funatsu, NHK Science & Technology Research Laboratories, Tokyo, Japan

In Paper 6.2, NHK Science & Technology Research Laboratories and Forza Silicon present a 133Mpixel 60fps 12b image sensor for 8K video. The pixel size in 0.18μm technology is 2.45×2.45μm^2. Front-end multiplexing analog readout circuitry and column-parallel successive approximation register ADCs are used.

6.3 A 45.5μW 15fps Always-On CMOS Image Sensor for Mobile and Wearable Devices **2:30 PM**

J. Choi, Samsung Advanced Institute of Technology, Suwon, Korea

In Paper 6.3, Samsung presents an always-on image sensor that enables smart sensing in addition to a photograph-shooting mode. Switchable always-on and photo-shooting modes are implemented using dynamic voltage-scaling and reconfigurable ADC circuits. The sensor has 640×480 pixels and consumes 45.5μW at 15fps in the always-on mode.

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6.4 Single-Shot 200Mfps 5×3-Aperture Compressive CMOS Imager **3:15 PM**

F. Mochizuki, Shizuoka University, Hamamatsu, Japan

In Paper 6.4, Shizuoka University presents a CMOS image sensor fabricated in a 0.11µm process with 5×3 apertures. The sensor performs single-shot and burst-readout image acquisition at a frame rate of 200Mfps employing image reproduction based on compressive sensing.

6.5 25.3µW at 60fps 240×160-Pixel Vision Sensor for Motion Capturing with In-Pixel Non-Volatile Analog Memory Using Crystalline Oxide Semiconductor FET **3:45 PM**

T. Ohmaru, Semiconductor Energy Laboratory, Kanagawa, Japan

In Paper 6.5, Semiconductor Energy Lab and the University of Tokyo propose a 240×160-pixel vision sensor with a motion-capturing function. The sensor has in-pixel non-volatile analog memory employing 0.5µm CAAC-IGZO FET/0.18µm p-ch Si FET technology to obtain differential data in a reference frame. It consumes 25.3µW at 60fps in a motion capture mode.

6.6 A 240Hz-Reporting-Rate Mutual-Capacitance Touch-Sensing Analog Front-End Enabling Multiple Active/Passive Styluses with 41dB/32dB SNR for 0.5mm Diameter **4:00 PM**

M. Hamaguchi, SHARP, Tenri, Japan

In Paper 6.6, Sharp presents a mutual capacitance touch-sensing architecture that achieves multiple active/passive styluses and multi-finger touch sensing at the same time through 60-inch and 13-inch displays, respectively.

6.7 A 2.3mW 11cm-Range Bootstrapped and Correlated-Double-Sampling (BCDS) 3D Touch Sensor for Mobile Devices **4:15 PM**

L. Du, University of California, Los Angeles, CA

In Paper 6.7, UCLA presents a 3D touch sensor SoC that uses an oscillator-based bootstrapped and correlated double sampling architecture for mobile applications. The 2.3mW 11cm 3D sensing system with 1cm resolution is achieved with small die area of 2mm^2.

6.8 A Pen-Pressure-Sensitive Capacitive Touch System Using Electrically Coupled Resonance Pen **4:45 PM**

C. Park, KAIST, Daejeon, Korea and Samsung Electronics, Suwon, Korea

In Paper 6.8, KAIST and Samsung present a pen pressure sensitive capacitive touch system with electrically coupled resonance pen that can replace costly EMR-based systems. The multi-TX scanning and charge demodulating integrator scheme achieves 49dB SNR with 1mmϕ 6b resolution pen pressure sensing.