## 5.1 A 60V Auto-zero and Chopper Operational Amplifier with 800kHz Interleaved Clocks and Input Bias-Current Trimming

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Precision operational amplifiers (opamp) with 30V supply operation have been widely used to support industrial, instrumentation, and other applications [1]. Most of them have been realized with BJT or JFET processes [1] to offer voltage noise PSD better than 10nV/√Hz and offset voltage drift better than 1μV/°C. Recently, opamps with similar specifications have become available using CMOS based processes [2-4], which can offer a cheaper wafer price. Auto-zeroing and/or chopping are used as essential techniques to reduce offset voltage drift and 1/f noise associated with CMOS input differential pairs. The switching action of those techniques, however, results in unwanted output ripples and glitches, which requires a post-filter and limits usable signal bandwidth. Increasing the switching frequency can extend the usable signal bandwidth, though it introduces DC errors such as offset voltage drift and input bias current. Maximum offset voltage drift of 0.02μV/°C and an input bias current of 600pA have been achieved [3], although the switching frequency at 60kHz limits the usable signal bandwidth. A high switching frequency of 333kHz has been achieved [2], while the maximum offset voltage drift and input bias current are 0.085μV/°C and 850pA, respectively.

This paper presents an auto-zeroed and chopped opamp operating in the 4.5 to 60V supply range, using a BCDMOS process based on 0.18μm CMOS technology. It achieves a maximum offset voltage drift of 0.015μV/°C, a noise PSD of 6.8nV/√Hz, and a 3.2MHz unity gain frequency, while dissipating 840uA of current. In addition to reducing modulated chopping ripples by combining auto-zeroing and chopping [5], glitches from the charge injection of input switches are mitigated by employing six parallel input stages with 800kHz interleaved clocks. It moves the majority of switching spectral energy up to 4.8MHz while leaving little spectral energy at 800kHz. Maximum input bias current is reduced from 2nA to 200pA by trimming during post-production testing, using an on-chip charge mismatch compensation circuit.

The auto-zeroed and chopped input transconductance amplifier, $G_{m1}$, is shown in Fig. 5.1.1, together with the timing diagram. It is composed of six identical channels in parallel, each of which is driven by individual and interleaved timing clocks. Each channel goes through pre-charging (PC), auto-zeroing (AZ), chopping (CHOP), and inverting-chop (CHOPB) phases as shown in the timing diagram. In the PC phase, two common mode level shift capacitors, $C_{LS}$, are connected in between the INP terminal and common mode buffer, CMBUF. The two $C_{LS}$ capacitors become floating voltage sources to provide the main transconductance amplifier, $G_{mmain}$, with a 1.6V common mode voltage in later phases, without creating a notch in the signal transfer function discussed in [6]. In the AZ phase, the input offset voltage of $G_{mmain}$ is sampled by auto-zero capacitors, $C_{AZ}$, and nulled by the auto-zero transconductance amplifier, $G_{maz}$, which otherwise results in modulated chopping ripples [5]. The differential output of $G_{mmain}$ gets connected to the signal path in the CHOP and CHOPB phases, and residual offset error and sampled noise from the AZ phase will be modulated by chopping. In contrast to two ping-pong channels [5], the proposed $G_{m1}$ with six channels reduces the power dissipated by auto-zeroing relative to that used for amplifying input signals. Four out of the six channels are in either CHOP or CHOPB phases, and contribute to amplifying the input signals. Meeting targeted noise PSD and signal bandwidth requires a transconductance value of $G_{mmain}$ and switch sizes in SWIN be four times smaller than those in [5]. The smaller input switches will create less glitch energy per switching event, which occur every 0.21μs (4.8MHz frequency). The energy of the glitches are shown at the bottom of the timing diagram, and are compared to those from [5], where the frequency is 800kHz.

Figure 5.1.2 shows the proposed input switching circuit, $SW_{IN}$, incorporating a charge mismatch compensation circuit. The four input switches ($SW_1$, $SW_2$, $SW_3$, and $SW_4$) have unwanted coupling capacitors with mismatch ($C_p$ and $C_p+\Delta C_p$). This will create an initial input bias current approximately equal to $2\bullet f_{CLK}\bullet\Delta C_p\bullet(CV_{DD}-CV_{SS})$, where $f_{CLK}$ is the switching frequency, and $CV_{DD}$ and $CV_{SS}$ are supply voltages of the inverters driving the four switches. The charge mismatch compensation circuit can generate compensating input bias current to offset the initial input bias current. It is composed of four coupling capacitors ($C_1$, $C_2$, $C_3$, and $C_4$) that have been intentionally added and are driven by additional inverters and adjustable supply voltages ($CV_{DD\_DACP}$ and $CV_{DD\_DACN}$). The compensating input bias current is controlled to be $2\bullet f_{CLK}\bullet C_0\bullet(CV_{DD\_DACP}-CV_{DD\_DACN})$, where $C_1$, $C_2$, $C_3$, and $C_4$ are assumed to be equal to $C_0$. The $CV_{DD\_DACP}$ and $CV_{DD\_DACN}$ are generated based on the $CV_{DD}$ and on 8b trimming code, $D_{TRIM}$. To determine the polarity, either $CV_{DD\_DACP}$ or $CV_{DD\_DACN}$ deviates from the $CV_{DD}$ according to the MSB of $D_{TRIM}$. The magnitude of the deviation is linearly changed with the rest of the bits, and the compensating input bias current will change by about 50pA with one LSB.

The overall opamp diagram is presented in Fig. 5.1.3, including the proposed input switching circuit, $SW_{IN}$, and the proposed input transconductance amplifier, $G_{m1}$, followed by second and output transconductance amplifiers, $G_{m2}$ and $G_{m3}$. The $D_{TRIM}$ is provided through a digital interface at post-production testing, after measuring the initial input bias current externally. The code of $D_{TRIM}$ is stored in on-chip fuse memory, which is read at power up. The input common mode regulator, CM-Reg, generates the $CV_{DD}$ and $CV_{SS}$ tracking to input common mode voltage ($V_{CM}$+1.5V and $V_{CM}$), to maintain constant charge injection in $SW_{IN}$. Thanks to input common mode level shifting with the $C_{LS}$, the $G_{mmain}$ and $G_{m2}$ can be supplied by a regulated 4.2V supply ($AV_{DD5}$). Under those internally regulated supplies, the $SW_{IN}$, $G_{mmain}$, $SW_{OUT}$, and $G_{m2}$ can be made of 5V CMOS devices, which offer better performance and smaller area than 60V DMOS devices. The input RC filter and clamping diodes are added to protect the devices in $SW_{IN}$ and $G_{mmain}$ against high voltage input transients. The clocks are generated under a regulated 3.6V supply voltage ($DV_{DD3}$), and a clock level shifter is used before the $SW_{IN}$.

The proposed design is fabricated as a standalone dual opamp in a die size of 1.5x2.1mm$^2$. The opamps are specified and tested under a supply voltage range from 4.5 to 60V, an input common mode range from negative supply rail up to 1.5V below positive supply rail, and temperature range from -40 to 125°C. Tested voltage noise PSD with unity gain configuration is shown in Fig. 5.1.4, achieving a flat 6.8nV/√Hz PSD at lower frequencies. The majority of the switching PSD is moved up to 4.8MHz, above the opamp unity gain frequency of 3.2MHz, with the use of the interleaved clocks. A narrow PSD is left at 800kHz due to mismatches among the six channels in $G_{m1}$. The level of this PSD varies for different opamp units as shown in the histogram. Additionally the PSD increases around 1.2MHz due to modulated auto-zero sampling noise. Lastly, noise from the output stage $G_{m3}$ shows up around 6.5MHz when the gain of $G_{m1}$ decreases, which hides the switching PSD at 4.8MHz. In Fig. 5.1.5, measured input bias current versus input common mode voltage, $V_{CM}$, is shown for 20 opamp units under 30V supply. The two figures are given to compare before and after the trimming, which is done at a single bias condition with 5.5V supply, 2.75V input common mode, and at room temperature. Looking at $V_{CM}$ equal to 15V in the figures, the trimming reduces the maximum input bias current from 500pA to 40pA. It increases up to 110pA when $V_{CM}$ approaches 0V or 28.5V, due to the lack of voltage headroom in the CM-Reg circuit. Raising the temperature to 85°C increases the input bias current to 130pA, mostly due to leakage current from ESD protection devices. Considering the spread in mass production and test error guard band, the maximum specified input bias current will be 200pA, which would have been 2nA without trimming. Other performance metrics are compared with previous work in Fig. 5.1.6.

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*References:*

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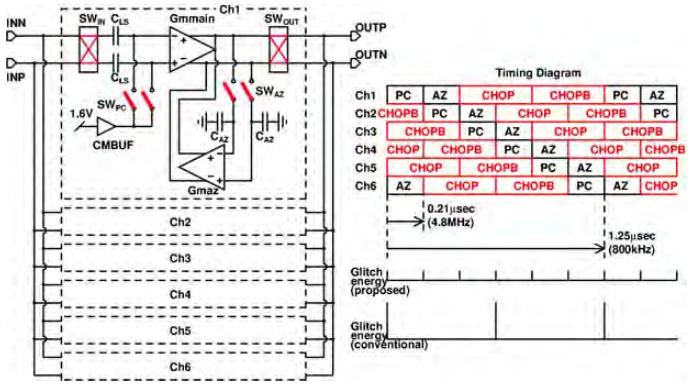


Figure 5.1.1: Input transconductance amplifier, $G_{m1}$, and timing diagram.

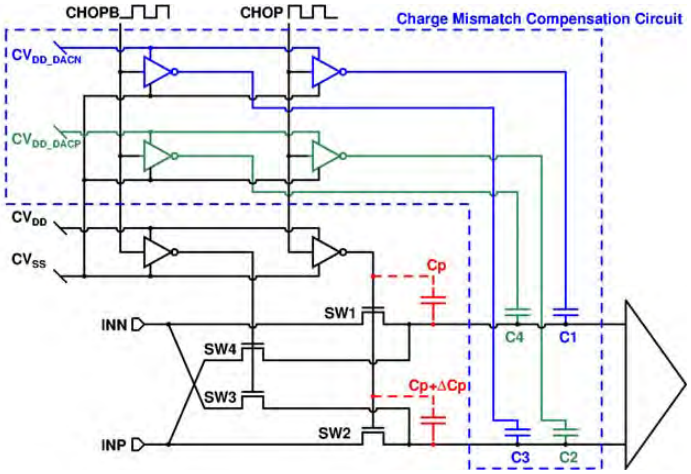


Figure 5.1.2: Input switching circuit, $SW_{IN}$.

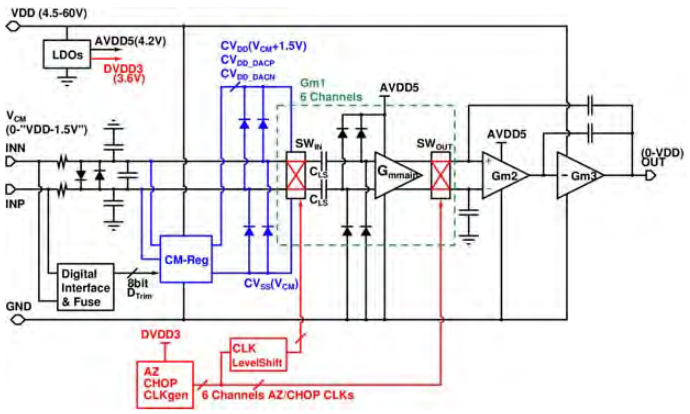


Figure 5.1.3: Overall operational amplifier diagram.

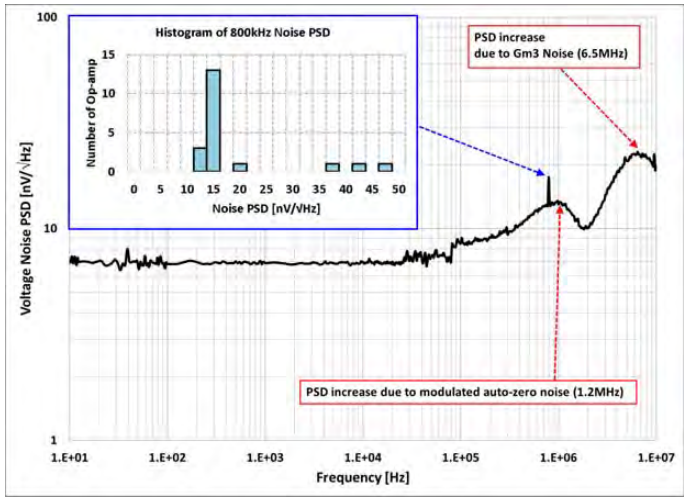


Figure 5.1.4: Voltage noise PSD and histogram of 800kHz noise PSD.

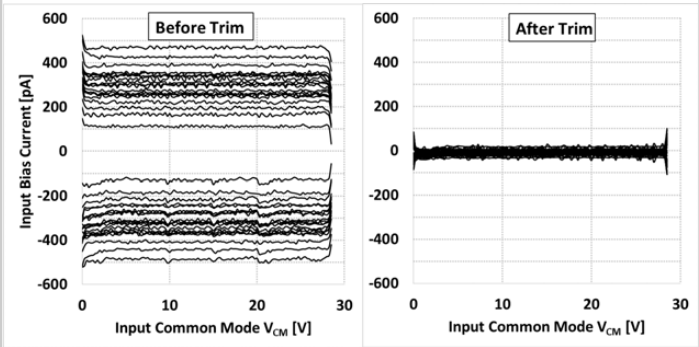


Figure 5.1.5: Input bias current vs. input common mode (before and after trimming).

| | This work | [1] | [2] | [3] | [4] |
|---|---|---|---|---|---|
| Year published | 2015 | 2011 | 2011 | 2012 | 2013 |
| Max. Operating supply [V] | 60 | 40 | 36 | 36 | 60 |
| Switching frequency [kHz] | 800/4800 | N/A | 333 | 60 | 100 |
| Max. Offset voltage [µV] | 4 | 120 | 25 | 5 | 4 |
| Max. Offset drift [µV/°C] | 0.015 | 1.000 | 0.085 | 0.020 | 0.015 |
| Max. Input bias current [pA] | ±200 | Not Shown | ±850 | ±600 | ±200 |
| Min. CMRR [dB] | 152 | Not Shown | 120 | 146 | 114 |
| Voltage noise PSD [nV√Hz] | 6.8 | 5.1 | 8.8 | 9.0 | 10.5 |
| Unity gain frequency [MHz] | 3.2 | 11.0 | 2.0 | 5.0 | 1.5 |
| Slew rate [V/µsec] | 1.2 | 20.0 | 0.8 | 3.8 | 0.45 |
| Current dissipation ($I_q$) [µA] | 840 | 1800 | 415 | 420 | 800 |
| Noise Efficiency Factor | 7.6 | 8.3 | 6.9 | 7.1 | 11.4 |

Figure 5.1.6: Performance comparison with previous work.

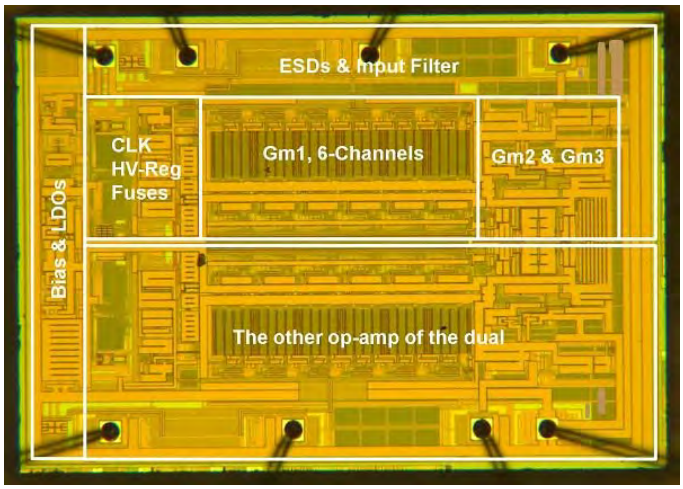


**Figure 5.1.7: Die micrograph of the proposed 1.5x2.1mm² dual opamp.**


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