3.6 A 10Gb/s Hybrid ADC-Based Receiver with Embedded 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS

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ADC-based receivers are currently being proposed in high-speed serial link applications to enable flexible, complex, and robust digital equalization in order to support operation over high loss channels [1-3]. However, the power dissipation of the ADC, as well as the digital equalization that follows, is a major concern for wireline receiver applications [3]. In this work, a hybrid ADC-based receiver architecture is presented that introduces innovations in both the ADC and the digital equalizer design. First, an analog 3-tap feed-forward equalizer (FFE) is efficiently embedded into a 6b time-interleaved SAR ADC, allowing for reductions in both ADC resolution and digital equalizer complexity. Second, significant power reduction is achieved by detecting reliable symbols at the ADC output and dynamically enabling/disabling the digital equalizer.

Figure 3.6.1 shows PAM2 BER bathtub curves for two backplane channels with different attenuations. The low-loss channel has an open eye with a voltage region over which a two-level slicer can reliably detect both '0' and '1' symbols at the required BER. Increased ISI from the high-loss channel causes the received eye to close with a slicer threshold set at the nominally optimal zero level, where significant errors are observed. In this case, typical receivers employ equalization on all received symbols to reduce ISI and open the eye to achieve the target BER. Certain received signal levels, however, have a very low probability of generating an error for a given symbol and do not necessarily require additional equalization. Our hybrid ADC-based receiver takes advantage of this to save power by employing a three-level detector with programmable thresholds that allows for reliable detection of both '0' and '1' symbols when the received signal falls outside the ambiguous region, and dynamically disables the digital equalizer on a per-symbol basis. For symbols in the ambiguous region that cannot be reliably detected, the digital equalizer is dynamically enabled to further remove ISI and achieve the target BER. Combining this technique with embedded FFE in the ADC allows for a significant reduction in digital equalizer power. The embedded FFE reduces the percentage of symbols in the ambiguous region [4].

The hybrid ADC-based receiver utilizes a 32-way time-interleaved 6b SAR ADC with embedded 3-tap FFE, as shown in Fig. 3.6.2. This 10GS/s converter has eight parallel sub-ADCs, each consisting of a front-end T/H clocked at 1.25GHz followed by four asynchronous unit SAR ADCs. A differential divide-by-four circuit is used with 5GHz complementary input clocks to generate the eight phases spaced at 100ps that clock the sub-ADC T/Hs. Digitally controlled capacitor banks, with a <0.4ps resolution and ~30ps range, are employed to calibrate timing mismatches in the clock distribution to the T/H blocks. The ADC includes calibration DACs for comparator offset, linear gain, and sampling clock skew. A switched-capacitor implementation allows for efficient embedding of the 3-tap FFE, which includes one pre-cursor and one post-cursor taps, into the capacitive DAC (CDAC) of the unit SAR ADCs [5]. In each unit ADC, the T/H_n input is sampled onto capacitor C_S to realize the main cursor with unity gain, while the post-cursor tap coefficient α_1 for the previous sample (T/H_{n-1}) and the pre-cursor tap coefficient α_{-1} for the next sample (T/H_{n+1}) are set with the CDAC weighting during the sampling phase.

Following the front-end ADC is a dynamically enabled digital equalizer, consisting of a 4-tap FFE and 3-tap DFE, which further equalizes any unreliable symbols. As shown in Fig. 3.6.3, latches are inserted in the equalizer computation path to only enable switching of the adders and multipliers if the digital threshold detector decides that an unreliable symbol is received. Additional multiplexers controlled by the threshold detector are placed after the loop-unrolled DFE digital slicers to select either the un-equalized reliable symbol from the ADC output or the further digitally equalized bits. While the additional digital threshold detector, latches, and multiplexers add a 19% power overhead relative to an always active equalizer, when combined with an ADC with embedded FFE the power savings are significant due to the relatively low activity factor of the equalizer computation path. In order to accommodate various channels, reconfiguration of the 4-tap FFE is possible with a main-cursor select control that allows all combinations ranging from all pre-cursor to all post-cursor equalization taps. A loop-unrolled architecture is utilized to meet the critical feedback timing paths of the digital 3-tap DFE [6], with a pipeline register bank inserted to improve the timing slack before the DFE selection multiplexers. The digital equalizer is fully synthesized using a digital standard-cell library and auto-placed-and-routed. To enable 10Gb/s operation, we use a 32-way time-interleaved parallel implementation where each slice is clocked at 312.5MHz.

Figure 3.6.7 shows a die micrograph of the hybrid ADC-based receiver, fabricated in a GP 65nm CMOS process. The core time-interleaved ADC and digital equalizer occupy 0.38mm^2 and 0.39mm^2, respectively, with other circuitry, such as the T/Hs, clock phase generation, reference buffers, and interface re-timing blocks bringing the total area to 0.81mm^2. 10Gb/s PRBS data is passed through various FR4 channels from a Centellax PCB12500 transmit module and the receiver digital equalizer output is fed back to the BERT for performance characterization. Here no transmit equalization is used, with the embedded FFE in the ADC and the dynamically enabled digital equalizer making up all the equalization in the system. Figure 3.6.4 shows timing margin bathtub curves for four FR4 channels with attenuations ranging from 20.9 to 36.4dB at the 5GHz Nyquist frequency, when an additional 1.5dB loss from the receiver board and package is included. First considered is the performance with only embedded ADC equalization activated, with both the embedded pre- and post-cursor FFE taps having a range of 33LSB and a resolution of 1.1LSB (Fig. 3.6.5). For this case, open eyes with timing margins exceeding 0.3UI are observed for the two lowest-loss channels. However, the two highest-loss channels require collaborative use of both the embedded and digital equalizers to obtain an open eye. When the digital equalizer is dynamically enabled on a per-symbol basis, timing margins of 0.2UI and 0.1UI are obtained for the 31.7 and 36.4dB channels, respectively, at a BER<10^{-10}. Figure 3.6.5 shows how digital equalizer power is saved with the hybrid-ADC receiver architecture for seven FR4 channels with attenuation ranging from 12.1 to 36.4dB. For channels with up to 25dB attenuation, the embedded equalizer alone opens the eye, translating into the digital equalizer being disabled 100% of the time and ideally all the digital equalizer power saved. When the power overhead due to the enable latches and threshold detector switching and leakage currents is considered, this slightly degrades to more than 80% power savings. For higher attenuation channels when the digital equalizer is enabled, the hybrid architecture achieves digital equalizer power savings of around 75% for up to 36.4dB channel attenuation. The ADC, T/Hs, and clock phase generation dissipate 79mW of power and the digital equalizer consumes 38mW, out of which more than 30mW can be saved by the dynamic-enabling of the hybrid architecture. Figure 3.6.6 compares this work with other ADC-based receivers operating near 10Gb/s [1-3]. The presented receiver is able to support operation over the highest loss channel among these designs, while also providing significant power savings in the digital equalizer.

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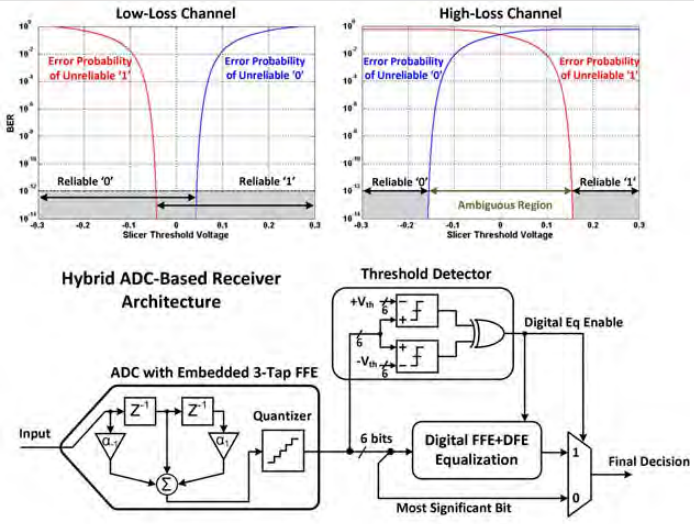

Figure 3.6.1: Receiver voltage margin BER bathtub curves with low- and high-loss channels, and block diagram of the hybrid ADC-based receiver.

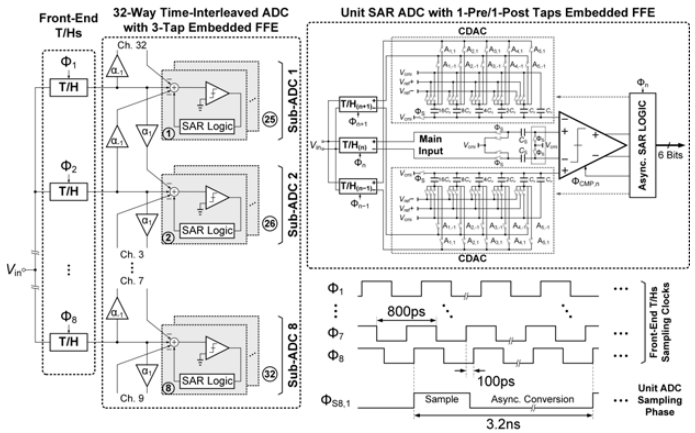

Figure 3.6.2: 32-way time-interleaved asynchronous SAR ADC with embedded 3-tap FFE.

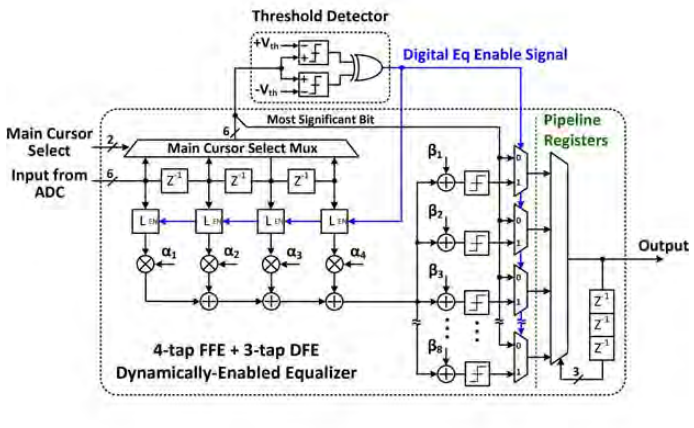

Figure 3.6.3: Dynamically enabled digital equalizer with 4-tap reconfigurable FFE and 3-tap loop-unrolled DFE.

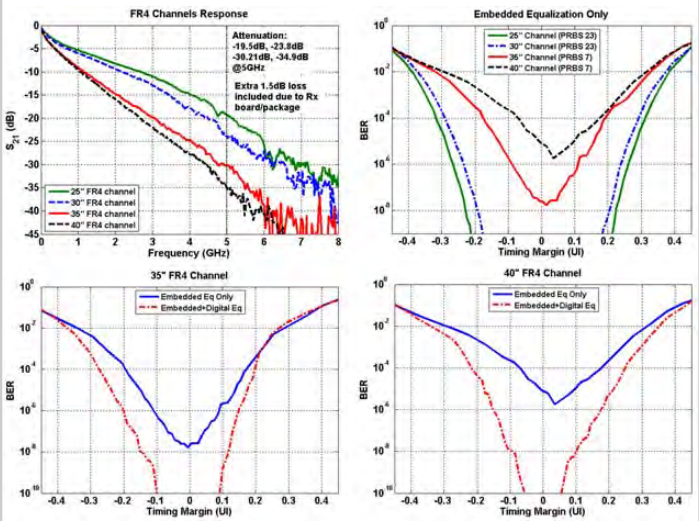

Figure 3.6.4: Receiver BER bathtub curves for 4 FR4 channels.

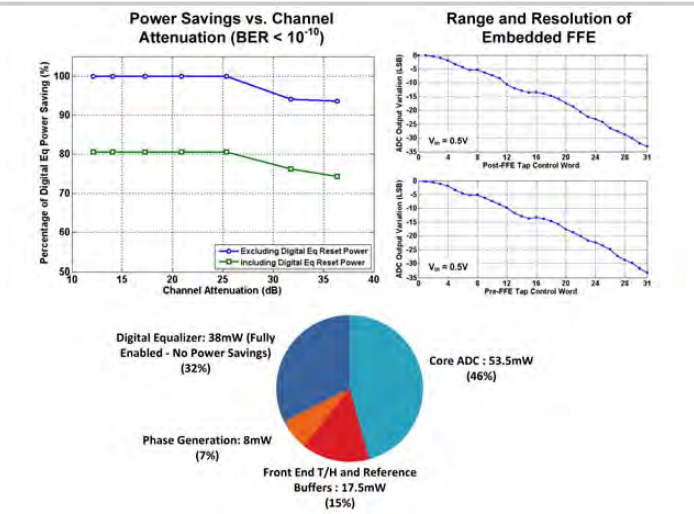

Figure 3.6.5: Hybrid ADC-based receiver digital equalizer power savings vs. channel attenuation (BER <10^{-10}), embedded 3-tap FFE range and resolution, and power breakdown.

Specification	[1]	[2]	[3]	This Work	
Technology	65nm	65nm	40nm	65nm	
Power Supply (V)	N/A	1.1	N/A	1	
ADC Structure	Flash	Variable V_{REF} Flash	Rectifier Flash	TI-SAR	
Pre-Equalization	4 taps FIR (@ TX)	HPF + 2 taps FFE	N/A	Embedded 3-tap FFE	
Post-Equalization	2-tap FFE + 5-tap DFE	5-tap DFE	Adaptive FFE+DFE	4-tap FFE + 3-tap DFE	
Sampling Rate (GS/s)	12.5	10	8.5-11.5	10	
Resolution (bit)	4.5	4	6	6	
ENOB (bit)	N/A	N/A	4.86	4.74	
Input Range (V_{pp})	N/A	0.6	N/A	1	
Area (mm^2)	0.45*	0.29	0.82	0.81	
Compensated Channel Loss	-24dB @ 12.5GS/s	-29dB @ 10GS/s	-34dB @ 10.3GS/s	-25.3dB @ 10GS/s	-36.4dB @ 10GS/s
ADC Power (mW)	150	93	195	79	
DSP Power (mW)	85	37	N/A	8	10
Power Efficiency (pJ/bit)	30.7*	13	19	8.7	8.9

* Includes both the TX+RX

Figure 3.6.6: Performance summary and comparison table.

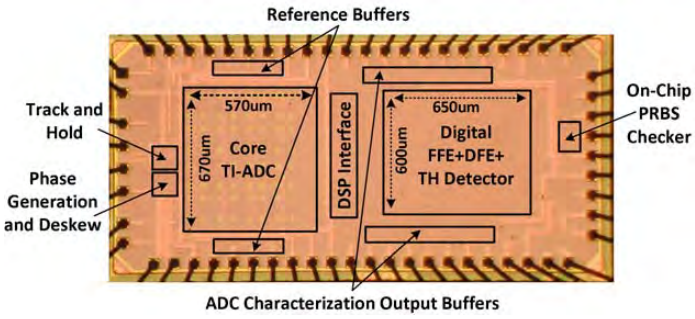

Figure 3.6.7: Die micrograph of the hybrid ADC-based receiver.

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