3.4 A 36Gb/s PAM4 Transmitter Using an 8b 18GS/s DAC in 28nm CMOS

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At data rates beyond 10Gb/s, most wireline links employ NRZ signaling. Serial NRZ links as high as 56Gb/s and 60Gb/s have been reported [1]. Nevertheless, as the rate increases, the constraints imposed by the channel, package, and die become more severe and do not benefit from process scaling in the same fashion that circuit design does. Reflections from impedance discontinuities in the PCB and package caused by vias and connectors introduce significant signal loss and distortions at higher frequencies. Even with an ideal channel, at every package-die interface, there is an intrinsic parasitic capacitance due to the pads and the ESD circuit amounting to at least 150fF, and a 50Ω resistor termination at both the transmit and receive ends resulting in an intrinsic pole at 23GHz or lower. In light of all these limitations, serial NRZ signaling beyond 60Gb/s appears suboptimal in terms of both power and performance. Utilizing various modulation techniques such as PAM4, one can achieve a higher spectral efficiency [2]. To enable such transmission formats, high-speed moderate-resolution data converters are required. This paper describes a 36Gb/s transmitter based on an 18GS/s 8b DAC implemented in 28nm CMOS, compliant to the new IEEE802.3bj standard for 100G Ethernet over backplane and copper cables [3].

The transmitter is composed of 20:1 multiplexers using a 1V power supply and the output DAC-driver utilizing a 1.5V supply (Fig. 3.4.1). The DAC is combined with the output driver [5] and is based on the current-steering topology. An NMOS segmented current DAC with shunt-peaked load is used to achieve the bandwidth required. In such a topology, the main trade-off is between the number of DAC coarse bits encoded through thermometer-weighted current cells and the number of fine bits encoded through binary-weighted current cells [4]. The higher number of coarse bits increases the number of current cells, which improves linearity but also introduces more parasitic capacitance at the DAC output and lowers the bandwidth. Furthermore it increases complexity and power consumption since each current cell requires its own multiplexer and routing to the output pads, regardless of its size. In this work, we segment the DAC into 2b thermometer-encoded and 6b binary-encoded current cells, resulting in a total of 9 current cells including 3 thermometer-weighted current cells and 6 binary-weighted current cells (Fig. 3.4.2). This reduces both parasitic capacitance and power consumption. However, the main drawback of increasing the number of bits that are binary-encoded is the higher requirement on the current cell matching at the border between binary-weighted current cells and thermometer-weighted current cells. The matching requirement to meet the DNL constraint and ensure monotonicity at bit n is described by the following equation:

$$I_n - (\sum_{k=0}^{n-1} I_k + I_{LSB}) < \frac{1}{2} I_{LSB}.$$

I_k is the current of the k^{th} bit. For each increase in the order of the highest bit that is binary-encoded, the matching requirement as a percentage of the current I_n rises by a factor of 2, increasing the size of the unit current cell by a factor of 4. This could result in significantly higher parasitic capacitance in the current source and a higher overall DAC area. To minimize the current cell size and realize the 2b thermometer 6b binary segmentation scheme, a coarse bit calibration circuit is implemented and will be described later.

As shown in [4], the linearity of the DAC depends on the output impedance of the current source. The third harmonic in full swing conditions can be approximated by $HD_3 = (R_L N/4|Z_{out}|)^2$ where $|Z_{out}|$ is the output impedance of the LSB current source, R_L the resistor load of the DAC, and N the total number of levels (in this DAC N = 256). At lower frequencies, Z_{out} is essentially resistive and beyond several GHz it becomes mostly capacitive due to the capacitance seen at the source node of the DAC switches (Fig. 3.4.2). The use of a cascode device M_c increases the output impedance at both low and high frequency and isolates the drain of the current source with significantly higher capacitance $C_{cs,}$ from the source of the DAC switch. Nevertheless, at very high frequencies, the cascode device is less effective and some of the capacitance C_{cs} appears at the output of the DAC through the cascode parasitic capacitances C_{gd}, C_{gs} and C_{ds} of M_c. Hence, it is important to ensure that C_{cs} is minimized by reducing the size of the current source as much as possible, yet ensuring the matching requirement for INL and DNL. The same calibration circuit helps achieve this goal.

Figure 3.4.3 describes the DAC coarse bit calibration circuit. The calibration is performed only for the 2 MSB bits that are encoded as thermometer-weighted current sources. This corresponds to 3 unit current cells $I_{6,}$ which are 64× the size of the LSB current cell. At start-up, the sum of all the current cells for lower bits for $\sum_0^5 I_k + I_{LSB}$ is compared to a reference current I_{ref}. I_{ref} is trimmed until its value is equal to $\sum_0^5 I_k + I_{LSB}$. In the next step, each I_6 current cell is connected to the calibration node and trimmed against I_{ref}. The coarse bit calibration circuit allows one to reduce the size of the unit current cell by 2×, reducing C_{cs} while meeting the DNL and monotonicity requirement for the 8b DAC.

The 20:1 multiplexer is entirely based on CMOS gates and serializes twenty 900Mb/s data streams into 18Gb/s. The highest clock frequency provided to the MUX is 9GHz hence the last stage of multiplexing is performed at half-rate, reducing the power consumption. The input of the DAC needs a common mode of around 1V to allow enough headroom for the current cells. Therefore, 18Gb/s level shifters using exclusively thin-oxide devices and resistive loads are designed to change the digital logic levels from 0 to 1V to 0.6 to 1.5V (Fig. 3.4.3). In this circuit, the device M_1 protects M_0 from over-voltage stress and the cross-coupled PMOS pair M_2 improves DCD of the 18Gb/s signals. The optimal swing to ensure that the current switches entirely in the DAC cell ($I_{Residue} < I_{LSB}$) and the switch transistor oxides are not over-stressed, is around 900mV. An analog servo-loop (Fig. 3.4.3) compares the logic level at the output of a replica circuit and ensures that the single-ended swing is maintained around the optimal value over PVT.

The phase of the 9GHz reference clock for the transmitter is controlled by a phase interpolator circuit with a resolution of 434fs (256 steps). Since the transmitter DAC has a finite settling time, some of the clock phase noise is converted into SNR, and hence needs to be minimized. The VCO phase noise is suppressed at the output by increasing the PLL bandwidth to around 8MHz. The noise contribution of all other PLL blocks becomes more significant at such bandwidths and needs to be reduced. A differential change pump with large bias current is used to reduce its output noise contribution. The loop filter uses a large integrator capacitance to reduce the zero resistor and its noise [6].

The transmitter is implemented in 28nm CMOS and occupies a total active area of 0.05mm^2. The DAC performance is characterized using a high-bandwidth spectrum analyzer. The SFDR exceeds 47dB up to 2GHz and 38dB up to the Nyquist frequency of 9GHz (Fig. 3.4.4). The THD exceeds 6b up to 3GHz and 5.5b up to the Nyquist frequency. The DAC bandwidth is measured and the loss is <2dB at 9GHz. The measured transmitter output random jitter is 109fs$_{rms}$. The dual mode transmitter can generate NRZ (18Gb/s) and PAM-4 (36Gb/s) format data streams achieving over 800mV$_{ppdiff}$ of full scale amplitude (Fig. 3.4.5). The ISI in the NRZ mode is below 3ps and the rise/fall time is lower than 11ps while the PAM-4 horizontal eye opening is about 0.67UI. The DAC enables equalization through the DSP. The power consumption of the transmitter is 84mW and the PLL and clock distribution is 60mW. A comparison table for the DAC has been provided in Fig. 3.4.6 and this design achieves the best FOM while occupying the smallest area among the compared designs. A chip micrograph is provided in Fig. 3.4.7. This 18GS/s 8b DAC enables more complex modulation and signal processing in future wireline applications.

Acknowledgment:
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References:

[1] Y.M. Greshishchev, et al., "A 56GS/s 6b DAC in 65nm CMOS with 256x6b memory," *ISSCC Dig. Tech. Papers*, pp. 194-196, Feb. 2011.
[2] A. Amirkhany, et al., "A 24Gb/s Software Programmable Analog Multi-tone Transmitter," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 999-1009, Apr. 2008.
[3] IEEE Standard 802.3bj-2011 "Physical Layer Specifications and Management Parameters for 100 Gb/s Operation over Backplanes and Copper Cables".
[4] C-H. Lin, et al., "A 12b 2.9GS/s DAC with IM3<-60dBc beyond 1GHz in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 74-75, Feb. 2009.
[5] J. Savoj, et al., "A 12-GS/s phase calibrated CMOS Digital-to-Analog Converter for Backplane Communications," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1207-1216, May 2008.
[6] B. Raghavan, et al., "A sub-2W 39.8-to-44.6Gb/s transmitter and receiver chipset with SFI-5.2 interface in 40nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 32-33, Feb. 2013.

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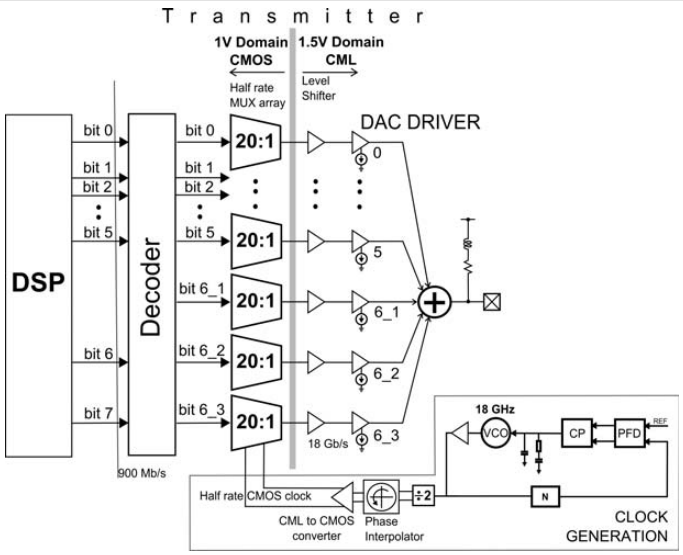

Figure 3.4.1: Block diagram of the transmitter and the clock generation PLL.

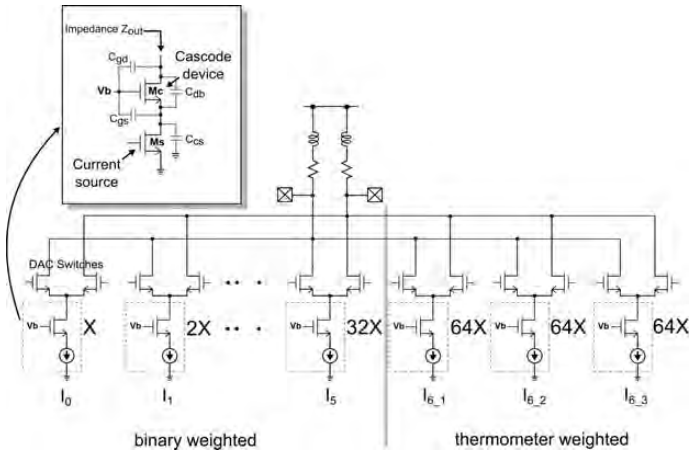

Figure 3.4.2: Diagram of the 8b DAC.

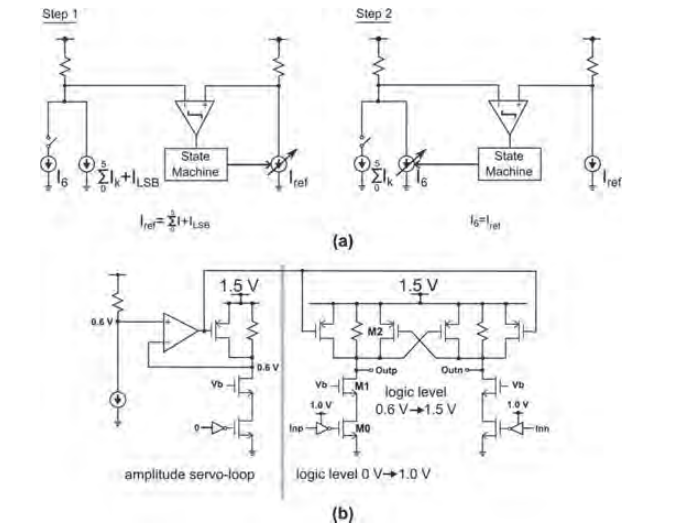

Figure 3.4.3: (a) Block diagram of the calibration circuit (b) Diagram of the 18Gb/s level shifter circuit and amplitude control servo-loop.

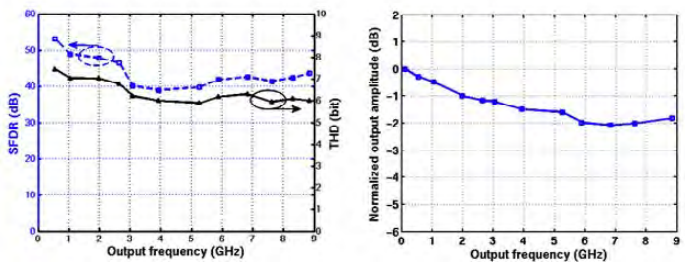

Figure 3.4.4: (a) Measured SFDR and THD vs. frequency (b) Normalized amplitude of the DAC vs. frequency (normalized to 800mV$_{ppdiff}$).

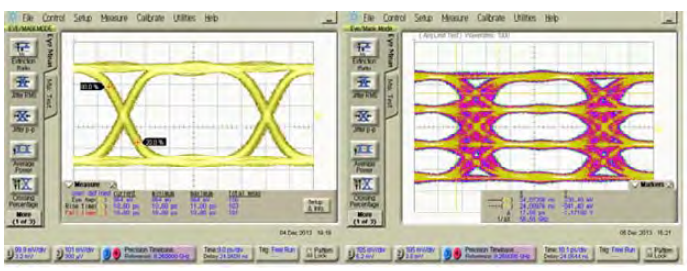

Figure 3.4.5: Dual mode operation: eye diagram for 18Gb/s (left) NRZ and 36Gb/s (right) PAM-4 without equalization.

	[5] JSSC 2008	[1] ISSCC 2011	This work
NOB	8	6	8
Fsample (GHz)	12	56	18
Data rate (Gb/s)	24	56	36
SFDR	51dB @ 0.75GHz 35dB @ 1.5GHz	43dB @ 1GHz 34dB @ 27GHz	52dB @ 0.7GHz 43dB @ 8GHz
Output Bandwidth (-3dB)	7.1GHz	40GHz(on wafer)	>9GHz
Power (mW)	190	750	84
FOM*	0.052pJ/conv.	0.14pJ/conv.	0.017pJ/conv.
Area (mm^2)	0.67x0.35	0.6x0.4	0.25x0.2
Supply	1V and 1.8V	1.1V and 2.5V	1V and 1.5V
Technology	90nm CMOS	65nm CMOS	28nm CMOS

*FOM $= \frac{Power}{2^{number\ of\ bits} \times 2BW}$

Figure 3.4.6: Comparison table with published (>10GS/s) digital-to-analog converters.

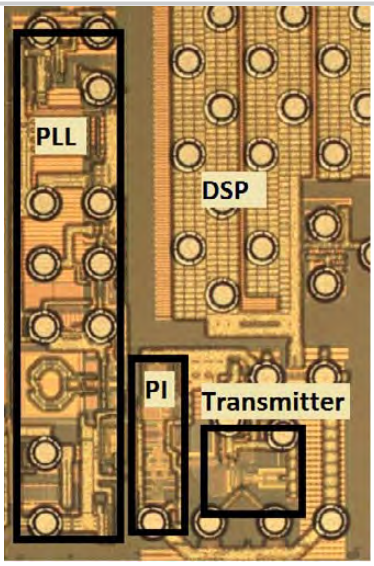

Figure 3.4.7: Die micrograph.

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