3.3 A 0.5-to-32.75Gb/s Flexible-Reach Wireline Transceiver in 20nm CMOS

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The introduction of high-speed backplane transceivers inside FPGAs has addressed critical issues such as the ease in scalability of performance, high availability, flexible architectures, the use of standards, and rapid time to market. These have been crucial to address the ever-increasing demand for bandwidth in communication and storage systems [1-3], requiring novel techniques in receiver (RX) and clocking circuits.

Figure 3.3.1 shows the transceiver architecture with reconfigurable clock generation consisting of two fractional-N LC PLLs per quad and a ring PLL per channel. Since the receiver and the transmitter (TX) require half-rate clock frequencies, the LC PLLs must cover a frequency range of 8 to 16.375GHz for data-rates of 16 to 32.75Gb/s. Lower data-rates are covered by dividing the frequency of the LC PLLs. Each PLL has two LC oscillators to provide a wide tuning range (>45% each) and these two PLLs have an overlap to allow two independent frequencies around 10G standards (covering 9.5 to 13.1GHz). The PLL consists of synchronized CMOS down-counter frequency divider and a programmable sigma-delta ($\Sigma\Delta$) modulator. The fractional PLL can be configured in either a MASH 1-1 (2^{nd} order) or MASH 1-1-1 (3^{rd} order) architecture by programming the ($\Sigma\Delta$) modulator. The frequency resolution is also programmable from 12 to 24 bits in steps of 4 bits.

Each LC PLL is followed by a passive wide-range 2^{nd} order polyphase filter (PPF) [4] for quadrature generation for high data-rates (>16.375Gb/s). For lower data-rates, a frequency divider divides the LC PLL frequency by two and produces quadrature signals. A multiplexer selects the PPF or the divider output depending on the speed of operation. The PPF circuit uses a two-stage constant-phase topology whose pole locations are chosen to track the frequency range of the preceding PLL. Poles are selected such that over PVT variations magnitude differences are within the tolerable range. A low-distortion linear buffer ensures low harmonic distortion to minimize I/Q error.

The differential high-speed I and Q clock signals are routed to the four transceiver channels. A long chain of CML buffers achieve good supply-noise immunity but suffer DC-offset accumulation and I/Q mismatch errors. A capacitive-degenerated CML buffer is inserted in every three buffer stages to attenuate DC gain as shown in Fig. 3.3.1. An additional duty-cycle correction (DCC) and I/Q calibration scheme is implemented in each transceiver channel to ensure good phase-interpolator (PI) linearity, which impacts receiver jitter tolerance margin [5].

Figure 3.3.2 shows the top-level block diagram of the clock DCC and I/Q correction scheme that can be used for both foreground and background calibrations. The duty-cycle distortion (DCD) is corrected for both I and Q phases prior to I/Q correction. The DCC and I/Q correction share the analog front-end with an auto-zeroed pre-amplifier to cancel out the offsets. The DCC correction scheme utilizes capacitor degeneration and 7b current DAC along with digital calibration logic. The correction range covers ±5ps of DCD, which is equivalent to 16% correction range at 16GHz clock with <150fs residual error. The correction part of I/Q error calibration uses a CML-based variable delay with error correction range of ±5ps. An offset-calibrated symmetrical XOR is used to sense I/Q error to achieve <180fs resolution.

Figure 3.3.3 shows the receiver, which consists of a 3-stage inductively peaked CTLE and a summer, and a 15-tap 1b unrolled DFE. To meet the high bandwidth requirement of the receiver over process corners and to minimize bandwidth variation, the load resistors of the CTLE and summer stages are calibrated against an external resistor. The summer circuit is the 4^{th} stage in a cascade of linear amplifier stages, necessitating stringent linearity requirements. To achieve high linearity, high current density for the summer input transistors is desired, resulting in reduced the headroom for the tail transistors over the PVT corners. To help ease this tradeoff between linearity and tail source headroom, source degeneration is added to the summer. The source degeneration resistance is implemented as a small array of NMOS transistors and is digitally programmable. The summer circuit utilizes a common-mode feedback bias (CMFB) circuit to stabilize its output common mode to a level suitable for the proceeding slicers. The CMFB loop detects the output common mode at the output of the summer through large resistors and controls the top PMOS gate.

A capacitively loaded summer (which sees 7 slicers and 15 differential pairs taps) requires high bandwidth on two paths; a forward path from CTLE to summer output, and a feedback path from DFE taps to summer output. Shunt peaking is used over a T-coil solution because in shunt peaking both forward and feedback paths see the same load and achieve very similar bandwidths whereas for a T-coil solution effective bandwidths are different between these two paths. Shunt peaking bandwidth extension ratio is usually a maximum of around 1.72×, which is enough to meet the bandwidth requirements of the summer.

The DFE circuit has 15 taps with the first bit unrolled. Note that in a generic DFE topology, the data (D) samples and the crossing (X) samples appear such that X lags D by 0.5 unit interval (UI), i.e., it uses late crossing. This configuration produces satisfactory results at higher data-rates. However, at lower data-rates, DFE tap feedback path can be completed in less than 0.5UI and there is not enough hold time for X samples. In order to resolve this issue, the DFE circuit is programmed such that for high data-rates X samples lag D samples by 0.5UI (i.e., D even (0°), X even (90°), D odd (180°), X odd (270°)) and for low data-rates, X samples lead D samples by 0.5UI (i.e., D even (0°), X odd (90°), D odd (180°), X even (270°)), as shown in Figure 3.3.4. The early/late crossing swap allows optimal link performance for all data-rates.

The transceiver is fabricated in a 20nm CMOS process and assembled in a flip-chip package. Figure 3.3.5(a) shows the receiver internal stressed eye scan at 32.75Gb/s over 10.4dB loss very short-reach (VSR) channel, and (b) at 28Gb/s 27dB loss long-reach (LR) channel. These measurements exclude package losses and account for crosstalk of 12 adjacent running lanes. Figure 3.3.5(c) shows the receiver jitter tolerance at 32.75Gb/s. The output transmit eye diagram at 32.75Gb/s utilizing PLL in integer N mode is shown in Fig. 3.3.5(d). Figure 3.3.6 summarizes the transceiver performance. Figure 3.3.7 depicts the die micrograph.

Acknowledgments:
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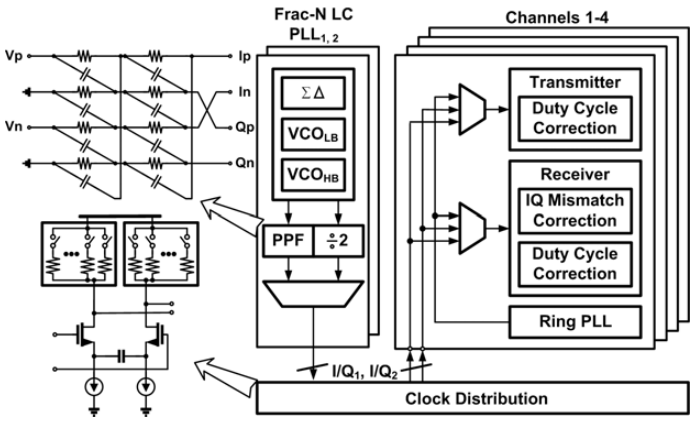

Figure 3.3.1: Transceiver architecture with two fractional-N LC PLLs.

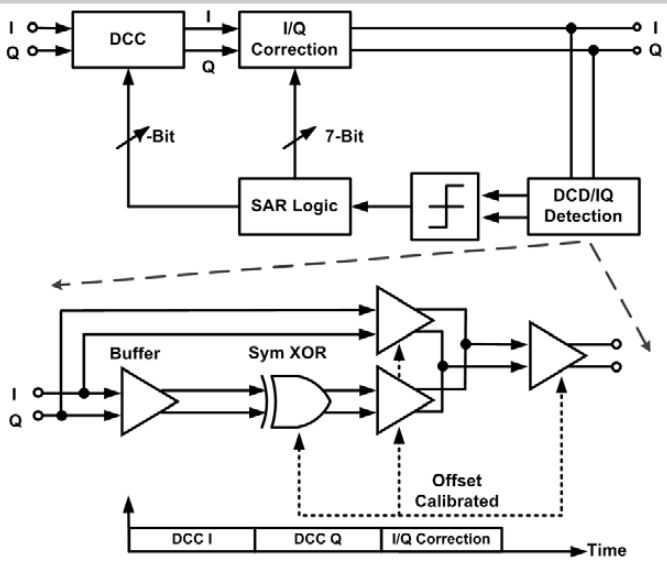

Figure Figure 3.3.2: Duty cycle and IQ error correction circuit.

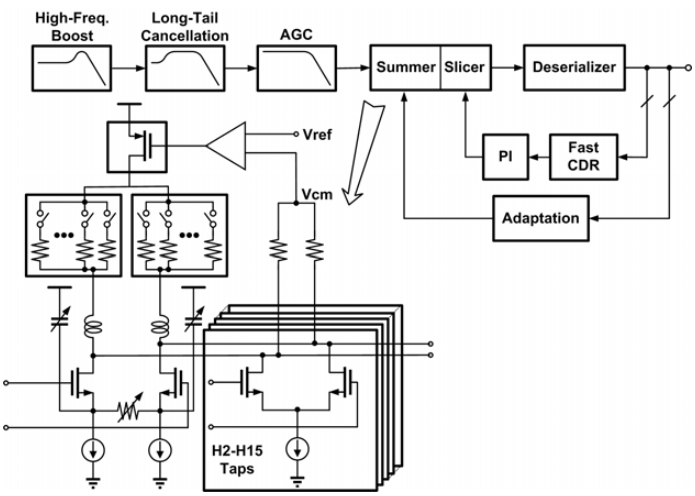

Figure 3.3.3: Receiver front-end for 15-tap, 1-bit speculative DFE topology.

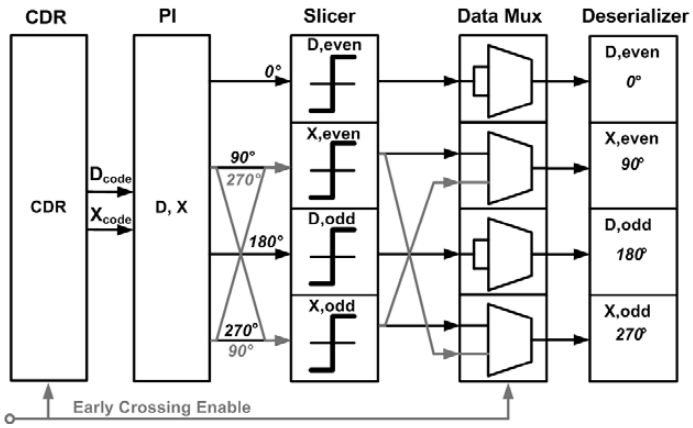

Figure 3.3.4: Early/Late (D/X Swap) crossing swap architecture.

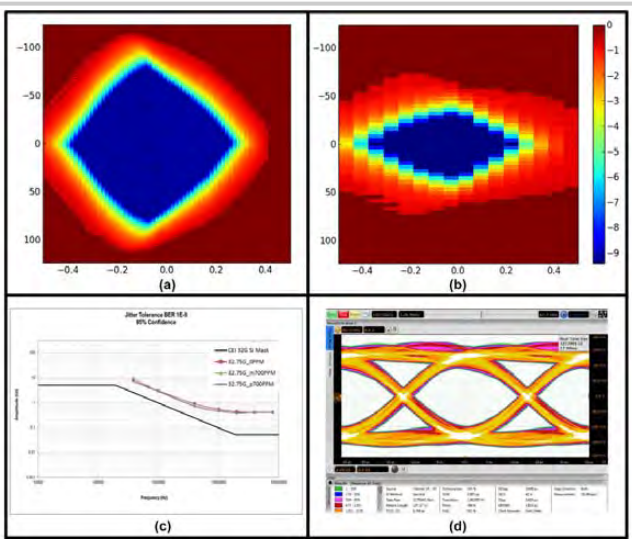

Figure 3.3.5: Receiver eye scan for (a) 32.75 Gb/s VSR and (b) 28Gb/s LR channels; (c) RX jitter tolerance and (d) transmit eye at 32.75 Gb/s.

Technology	CMOS 20nm SOC
Power Supply (V_{dd}, V_{aa}, V_{tt})	0.95V, 1V, 1.2V
Frequency range	500Mb/s – 32.75Gb/s
Quad area	2.700mm × 2.213mm
LC PLL range	8-16.375GHz
Ring PLL range	2-6.25GHz
TX PRBS7 jitter w/ LC PLL at 32.75Gb/s	TJ: 6.76ps, RJ: 205fs, DCD: 42fs
Fractional-N Mode	TJ: 6.85ps, RJ: 214fs, DCD: 44fs
TX jitter w/ ring PLL at 12Gb/s	TJ: 11.7ps, RJ: 621fs, DCD: 350fs
32.75Gb/s RX JTOL @ 100MHz	0.4UI
Max channel loss at 28Gb/s	27 dB
Measured BER at 28Gb/s	$< 10^{-15}$
Max channel loss at 32.75Gb/s	10.4 dB
Measured BER at 32.75Gb/s	$< 10^{-15}$
Power at 28Gb/s with DFE	785mW/ch

Figure 3.3.6: Performance summary.

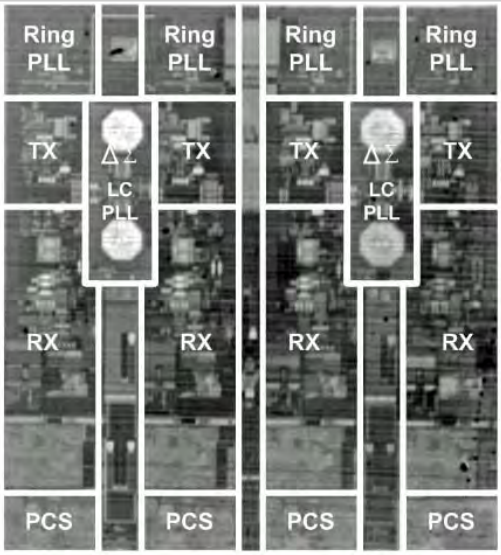

Figure 3.3.7: Die micrograph (2.700×2.213mm²).

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