3.2 Multi-Standard 185fs$_{rms}$ 0.3-to-28Gb/s 40dB Backplane Signal Conditioner with Adaptive Pattern-Match 36-Tap DFE and Data-Rate-Adjustment PLL in 28nm CMOS

Takashi Kawamoto[1], Takayasu Norimatsu[1], Kenji Kogo[1], Fumio Yuki[1], Norio Nakajima[2], Masatoshi Tsuge[2], Tatsunori Usugi[2], Tomofumi Hokari[2], Hideki Koba[2], Takemasa Komori[2], Junya Nasu[2], Tsuneo Kawamata[2], Yuichi Ito[2], Seiichi Umai[2], Jun Kumazawa[2], Hiroaki Kurahashi[2], Takashi Muto[2], Takeo Yamashita[2], Masatoshi Hasegawa[2], Keiichi Higeta[2]

[1]Hitachi, Tokyo, Japan,
[2]Hitachi, Kanagawa, Japan

As processing and network speeds are accelerated to support data-rich services, the bandwidth of backplane interconnects needs to be increased while maintaining the channel length and multi-rate links. However, channel losses and impedance discontinuities increase at high data-rates, making it difficult to compensate the channel. In this work, we target serial links from auto-negotiation in 100G-KR4 of 0.3Gb/s to 32GFC of 28.05Gb/s in 40dB backplane architecture [1-3]. To achieve this challenge, there are two key techniques. First, we introduce a 36-tap decision-feedback equalizer (DFE) to cancel reflections due to connectors because these reflections close the eye. To operate the 36-tap DFE, we need to fix a CDR lock-point and calculate 36-tap coefficients accurately. Thus, we develop a pattern-captured CDR with a 4b pattern filter to fix the lock-point, and a 3b pattern-matched adaptive equalizer (AEQ) to optimize 36 tap coefficients. These techniques enable our chip to compensate 40dB channel loss. Second, we target 100G-KR4/40G-KR4/10G-KR/25G-KR and 32GFC/16GFC/8GFC/4GFC. To operate across a wide range of data-rates, from 0.3 to 28.05Gb/s, with low jitter, we develop a PLL architecture with two LC-VCOs and one ring VCO with a data-rate-adjustment technique by controlling an LDO. Our test chip is fabricated in 28nm CMOS. Our signal conditioner is the demonstration to achieve the BER <10^{-12} PRBS31 at 100G-KR4 in a 40dB chip-to-chip backplane with two connectors by using the 36-tap DFE to cancel the reflection and to operate across a wide range of data-rates from 0.3 to 28.05Gb/s.

Figure 3.2.1 shows a backplane architecture and characteristics of a measured channel that consists of backplane, packages, sockets, and daughter boards. A 40dB total loss and length of reflection due to connector is same as those of target backplane architecture. There are many reflections due to impedance mismatch of a DC block capacitor, packages, vias, and connectors as shown in a time-domain reflectometer (TDR). These reflections can be cancelled only by using a DFE. In order to cancel large reflections due to the backplane connector, we introduce a 36-tap DFE.

Figure 3.2.2 shows the top-level overview. To reduce output jitter, both RX and TX have a half-rate PLL. The RXPLL generates I/Q 4-phase clock. The TXPLL takes the role of a jitter filter to cut off the jitter in the recovered clock. In the data-path, a continuous-time linear equalizer (CTLE) and 36-tap DFE, whose tap coefficients are determined by the AEQ, compensate a channel loss. The recovered clock is divided by 64 to use as the reference clock of the TXPLL. An 8:1 multiplexer (MUX) generates pre/main/post1/post2 4-phase data for a 4-tap feed-forward equalizer (FFE). A rate-detect circuit recognizes the data rate and then configures the blocks for a given data-rate if the rate is changed. For low-speed links <4.0Gb/s such as the auto-negotiation in the 100G-KR4, the bypass path is selected. This architecture supports a wide data-rate range from 0.3 to 28.05Gb/s.

Figure 3.2.3 shows a block diagram of the 36-tap DFE, pattern-matched AEQ, and pattern-captured CDR. The data feeds even/odd 3-to-36 tap current-summer DFE and tap-1 and tap-2 loop-unrolled DFE [2]. The 36-tap DFE has design issues related to the delay of the current-summer DFE and optimization of tap coefficients. First, if the delay of the current-summer DFE is large, the ISI cannot be cancelled sufficiently. To reduce this delay, the summed current of tap coefficients 3 to 36 (H3 to H36) are added to the data. Second, if the tap coefficients are not accurate, the ISI and reflections cannot be cancelled sufficiently. To optimize the tap coefficients, it is necessary to fix the CDR lock-point and balance tap coefficients between data patterns. For a long trace channel, a data edge is affected by the data pattern due to residual ISI. The transitions in the Nyquist patterns of 01 and 10 may not cross over the threshold voltage (+/-W) due to a lack of equalization. Thus, the CDR cannot use these patterns for phase detection. If the CDR does detect all data edges, the CDR lock-point varies, causing insufficient DFE equalization due to large variation of the tap coefficients [4]. To avoid this problem and reduce the variation of the lock-point, the CDR should select captured data patterns. Moreover, the CDR captures the data before the tap coefficients are added to the data. Thus, if data of tap-1 and tap-2 is 01 and 10, the CDR may fail to capture the data or the CDR lock-point variation is large due to the residual ISI. Thus, the CDR should capture the data when the data of taps 1 and 2 is 00 and 11. To solve these issues, we develop a pattern-captured CDR by using a pattern filter. The CDR captures 0001 pattern to fix the lock-point. The pattern-captured CDR with 4b pattern filter reduces the variation of the lock-point from 10 to 1.7ps and the residual ISI from 20 to 9ps for a 40dB channel.

Figure 3.2.4 shows the developed RXPLL architecture that incorporates two LCVCOs and one ring VCO (RVCO) with a data-rate-adjustment technique using LDOs. The RVCO oscillates from 2 to 11GHz, covering from 4 to 22Gb/s. The LC-VCO25G oscillates from 22 to 26GHz and 4-phase half-rate clocks are generated by a divide-by-2. The LC-VCO25G covers from 22 to 26Gb/s in half-rate mode and from 11 to 13Gb/s in full-rate mode. The LC-VCO28G covers from 26 to 29Gb/s and from 13 to 14.5Gb/s. To solve the trade-off between 4GHz frequency range and 0.2ps$_{rms}$ jitter, we develop a data-rate-adjustment technique by controlling the LDO. The LC-VCO oscillation frequency can be controlled by the LDO output voltage. As the LDO output voltage is lowered, the amplitude of oscillation signals reduce, increasing the frequency of oscillation. The LC-VCO achieves the 4GHz frequency range with 4b coarse tuning and LDO control technique from 0.45 to 0.65V. The LC-VCO frequency range is increased from 1.8 to 4.5GHz by the data-rate-adjustment technique. There are several combinations between LDO output voltage and LC-VCO bands in which the PLL can lock. After the LC-VCO and LDO are calibrated, the lowest LDO output voltage is selected to save power.

Figure 3.2.5 shows measured results of a 40dB backplane between trace BERT-to-chip at 100G-KR4 PRBS31. The BER is <10^{-12} at TX output signal when the equalization budget is 18dB CTLE, 12dB FFE, and 10dB DFE. When the number of the DFE taps is less than 36, the BER is not <10^{-12} because the large reflections due to the connectors are not cancelled. The tap-1 coefficient becomes large to equalize the ISI. The tap-31 and tap-32 coefficients are large to cancel the reflection due to the far-side connector. We achieve <185fs$_{rms}$ random jitter from 7MHz to 10GHz.

Figure 3.2.6 shows measurement results of the 40dB chip-to-chip backplane trace at 100G-KR4 PRBS31. The BER is <10^{-12}. Our signal conditioner can achieve 40dB loss compensation at 25.78125Gb/s and cover data rates from 0.3 to 28.05Gb/s. The chip area is 5.5×4.6mm^2 shown in Fig. 3.2.7.

References:

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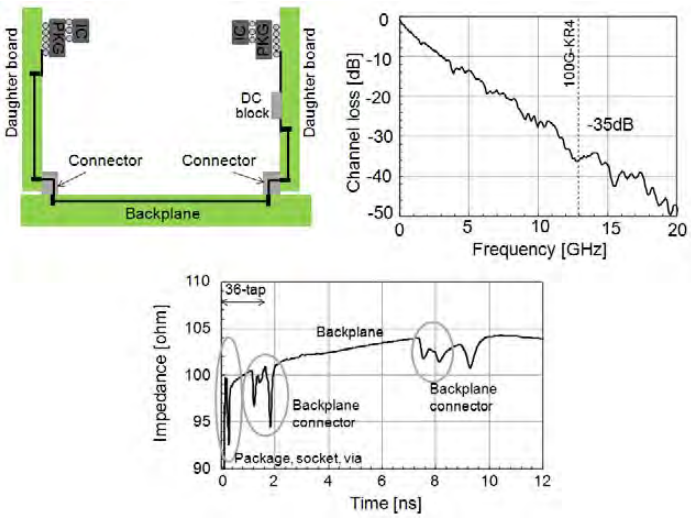


Figure 3.2.1: Target backplane architecture and channel characteristics.

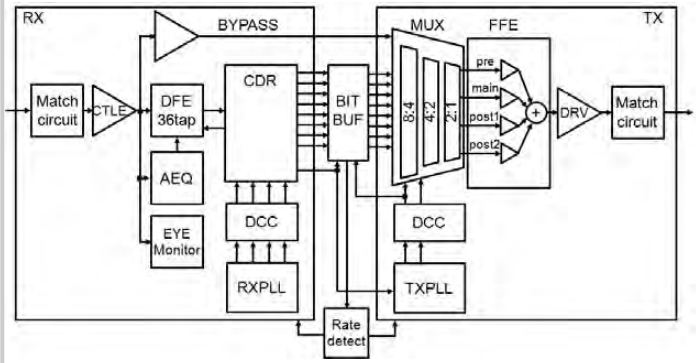


Figure 3.2.2: Top-level overview of backplane signal conditioner.

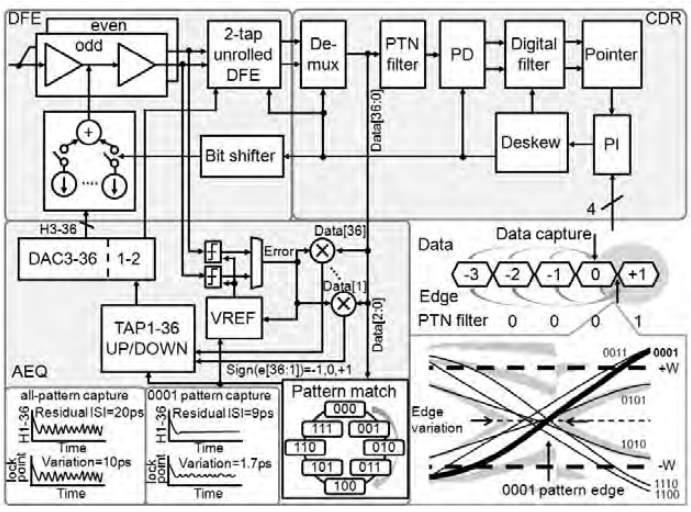


Figure 3.2.3: 36-tap DFE, pattern-matched AEQ, CDR overview.

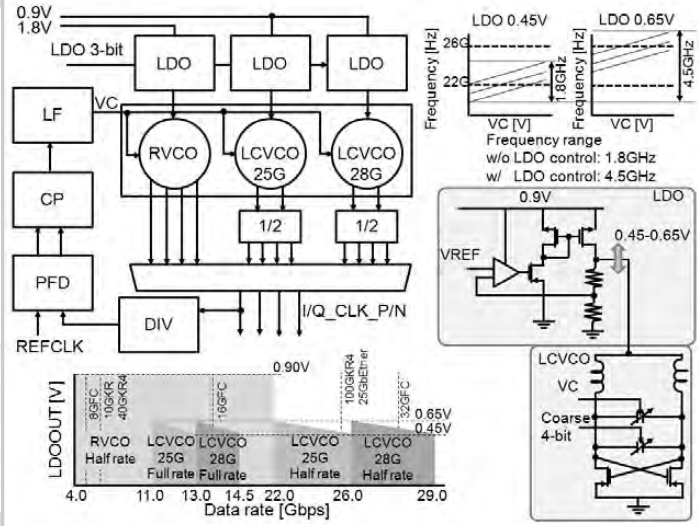


Figure 3.2.4: RXPLL overview and schematic of LDO and LC-VCO.

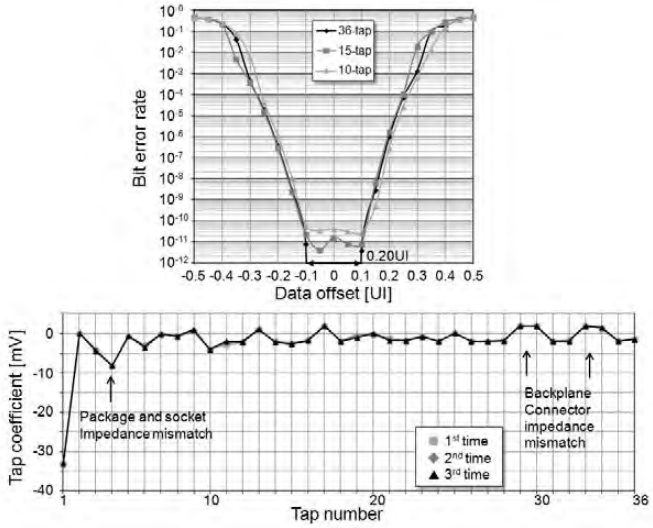
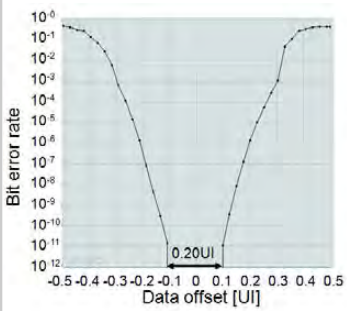


Figure 3.2.5: Measured BER and tap-coefficients in BERT-to-chip 40dB backplane trace.



Technology	28nmCMOS
Supply voltage	0.9/1.8V
Loss of Nyquist	40dB (25.78125Gbps)
Data rate	0.3 – 28.05Gbps
TXPLL bandwidth	0.5 – 10MHz
Output jitter	185fsrms
Power	25.1mW/Gbps
Chip area	5.4 x 4.6 mm/8lane

Figure 3.2.6: Measured BER and performance summary.

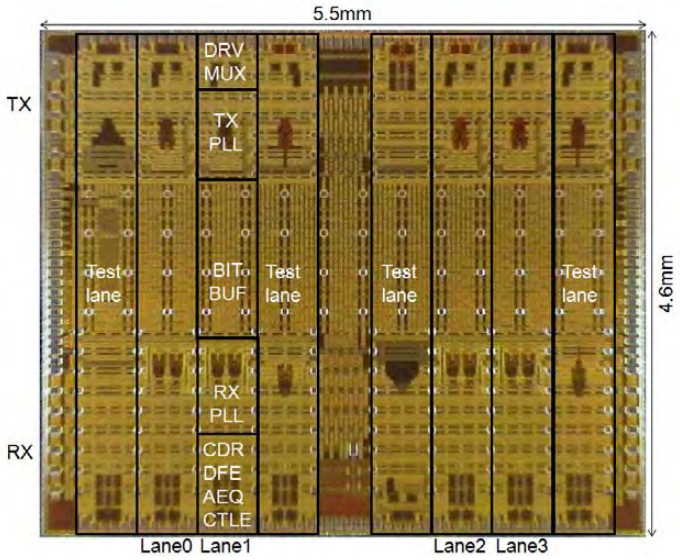


Figure 3.2.7: Chip micrograph.

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