3.1 A 28Gb/s Multi-Standard Serial-Link Transceiver for Backplane Applications in 28nm CMOS

Bo Zhang, Karapet Khanoyan, Hamid Hatamkhani, Haitao Tong, Kangmin Hu, Siavash Fallahi, Kambiz Vakilian, Anthony Brewster

Broadcom, Irvine, CA

Rapid internet traffic growth has fueled the demand for bandwidth in metro networks and data centers and pushed the serial link data rate into 25Gb/s territory, populated by such electrical interface as OIF CEI-25G, CEI-28G [1], IEEE 802.3bj 100G-KR4. To cope with severe channel impairments at 25Gb/s with up to 30dB loss at Nyquist, a feed-forward equalizer (FFE)/decision feedback equalizer (DFE) based transceiver without power-hungry analog-to-digital converter (ADC) provides robust performance. This work presents a low-power and area-efficient transceiver that employs a 14-tap adaptive DFE at the receiver (RX) and a 5-tap FFE at the transmitter (TX) for multi-standard applications up to 28Gb/s in 28nm CMOS.

The transceiver block diagram is illustrated in Fig. 3.1.1. In the RX, after an inductor-shunted termination that overcomes electrostatic discharge (ESD) diodes for better return loss (RL), a programmable continuous-time linear equalizer (CTLE) followed by a four-stage variable gain amplifier (VGA) provide moderate equalization and maintain a proper signal level before the DFE. A quarter-rate 14-tap DFE features an unrolled Tap_1 to further equalize the channel loss and reflection without enhancing channel noise and crosstalk. Six phase interpolators (PI) generate quarter-rate clocks for the data, phase, and LMS (error) channels. A delay locked loop (DLL) produces eight clock phases for PI to provide better phase tracking between data and phase clocks. The demultiplexer (DMUX) sends deserialized data/phase/error information into the digital side for CTLE/VGA/DFE adaptation and timing recovery (TR). Multiple calibrations, such as resistance and VGA/summer/slicer offsets, are built in to further improve the performance. The TX adopts a half-rate multiplexer (MUX) topology with duty-cycle distortion (DCD) correction and a full-rate source-series-terminated (SST) driver with 5-tap FFE. One common phase-locked loop (PLL) utilizes an LC voltage-controlled oscillator (VCO) to achieve a wide operation range and excellent phase noise performance. It sends quarter-rate clocks to four RXs and half-rate clocks to the TX clock generator. A TX clock generator with a PI for loop-timing mode produces TX multiplexing clocks and distributes them to four TXs.

In the RX, a single-stage two-zero peaking CTLE shown in Fig. 3.1.2 provides adequate analog equalization at low and high frequencies. It uses a two-path summing scheme, the fast path realizing high-frequency peaking with a degenerated small RC and the slow path using a large RC lowpass filter in front, which obtains low-frequency peaking after being subtracted from the fast path without impairing RL. Both peaking strengths are independently programmable. The total equalization at high frequency and low frequency can be 8dB and 6dB, respectively.

A half-rate RX solution with unrolled Tap_1 [2-5] is the popular choice in high-speed DFE design. Tap_2 summing timing in an unrolled Tap_1 scheme becomes a performance-limiting factor due to an additional stage for Tap_1 MUX selection, typically a 4-stage delay. Dedicating one summing unit for each slicer path [4], including tap 2 and beyond, can relax timing but creates a large overhead for signal routing on multiple tap summing, mismatch between summers, etc. In this work, we adopt a quarter-rate topology to double the slicer regeneration time, ease the clock distributions and alleviate the critical Tap_2 summing timing constraint to three stages and to meanwhile balance the timing margin for other taps. The 14-tap DFE data-path block diagram is shown in Fig. 3.1.3. The VGA output feeds into four identical baud-period (T_s)-spaced channels of a, b, c, and d. The Tap_1 summing stage and slicer are combined into a reference subtraction-based slicer that eliminates one-stage delay with the cost of a fixed slicer-input common-mode voltage. The current-summing circuit will shift down the output common-mode voltage with tap weight increase. The tap summing is split into two cascaded stages: sum_1 and sum_2. Sum_1 handles tap 3 to 14 summing without common-mode compensation. Sum_2 (Fig. 3.1.3) is used for Tap_2 summing, and constant common-mode voltage is realized by steering unused Tap_2 digital-to-analog converter (DAC) currents to a biased pair with bleeding currents at the output. The Tap_2 summing timing constraint is down to $T_{dc2q} + T_{mux} + T_{sum2} < 1.5T_s$, where T_{dc2q}, T_{mux}, and T_{sum2} are the delays of slicer/latch clock to Q, MUX, and sum_2, respectively, other tap constraints still meet $T_{lc2q} + T_{sum1} + T_{sum2} < 1.5T_s$ or more, and where T_{lc2q} and T_{sum1} are the delay of the latch clock to Q and sum_1 respectively. Each sum_2 output drives five slicers: two for data, two for phase, and one for LMS path, with independent clocks from PIs for flexibility of TR mode and an eye-monitoring function. The slicer (Fig. 3.1.3) has a built-in range-extended offset DAC for three purposes: 1) offset calibration for the summer/slicer; 2) additional Tap_1 weight for DCD compensation; and 3) calibrated slicer selection by setting all other channel data slicer DACs to the maximum positive or negative value during offset calibration. The outputs of each Tap_1 MUX and following latch are used as multiple inputs, e.g., Q_{1a} for the channel b Tap_1 selection, Tap_{2c} and Tap_{3d} and Q_{2a} for Tap_{4a}, Tap_{5b}, and Tap_{6c}. Then CMOS MUXs are used for floating tap 7-14 selection from the recovered data range from 7 to $26T_s$. Early latch outputs are used to relax timing constraint for floating taps.

To ensure the half-rate TX performance, we implement automatic DCD correction circuit within current-mode-logic (CML)-to-CMOS clock converter (D2C), shown in Fig. 3.1.4. It senses the clock DCD with a high-gain low-pass filter and injects a correcting current into the D2C circuit to eliminate duty-cycle error. Five T_s-spaced data as precursor, main, and post-cursor 1, 2, and 3 are generated in the half-rate domain by 2:1 MUXs using CMOS logic, a half circuit shown in Fig. 3.1.4. Sharing an on-chip 1V low-dropout regulator (LDO) with a 2:1 MUX, the full-rate SST driver is constructed by a group of switching resistor unit drivers, which provides stable termination resistance, small common-mode distortion and immunity to digital noise. In each unit driver, there are two R_u resistors in series with PMOS and NMOS switches and input enable/selection logic, in which only one switch is on at a time. The 50Ω main driver is composed of 55 unit drivers. Precursor and post-cursor 1 share part of the main driver units by using the input selection MUX to reduce total driver load and post-cursor 2 to 3 to have their own units with fewer unit drivers. The 5-tap FFE is realized by switching between main and pre-cursor/post-cursor 1 and switching on/off post-cursor 2 to 3. A programmable resistor array at the driver output is used to adjust output amplitude, and serial inductor peaking extends the driver bandwidth and achieves better return loss.

The PLL is common for the four RX/TX pairs shown in Fig. 3.1.5. A transformer-based LC-VCO is implemented to double the LC-VCO tuning range. The inductor is replaced by a transformer. When the inner turn of the transformer is shorted, the effective inductance in the primary turn is reduced for high-frequency oscillation, while the Q drop due to the mode switch is not critical. When the inner turn is open, the primary turn shows its intrinsic inductance for low-frequency oscillation. This VCO consumes less power due to high inductance at low frequency compared to a fixed inductor topology.

The transceiver is fabricated in 28nm standard CMOS as part of gearbox and switch chips and tested against multiple 25Gb/s and legacy standards. It passes RX/TX RL templates and the 2kV human-body model (HBM) ESD test in a 60×60mm² package. For a 1m backplane with 40dB Nyquist insertion loss (excluding package) at 25.78Gb/s PRBS31 data pattern with eight channels operating at same time, the RX is measured at BER $<10^{-12}$ with a 23% eye margin; an internal recovered eye is captured in Fig. 3.1.6 (upper). The TX has a measured total jitter of 8.4ps under BER = 10^{-15} and DCD of 50fs at 28.125Gb/s PRBS9 data pattern in Fig. 3.1.6 (bottom). The VCO tuning range is from 20 to 29GHz with jitter of $0.23ps_{rms}$ at 28.125GHz. The transceiver consumes 295mW (analog only) from a 1V supply (except TX LDO at 1.25V) per RX/TX, which is the lowest among published results for similar data-rate [2,3,5]. The die area is 0.62mm² per RX/TX, and a micrograph of four transceivers with PLL is shown in Fig. 3.1.7.

References:

[1] OIF CEI-25G-LR OIF2008.161.12, CEI-28G-SR OIF2008.029.12, "CEI-25G-LR Long Reach Interface" and "CEI-28G-SR Short Reach Interface."

[2] D. Cui, *et al.*, "A Dual 23Gb/s CMOS Transmitter/Receiver Chipset for 40Gb/s RZ-DQPSK and CS-RZ-DQPSK Optical Transmission", *ISSCC Dig. Tech. Papers*, pp. 330-331, Feb. 2012.

[3] J. Bulzacchelli, *et al.*, "A 28-Gb/s 4-Tap FFE/15-Tap DFE Serial Link Transceiver in 32-nm SOI CMOS Technology", *J. Solid-State Circuits*, pp. 3232-3248, Dec. 2012.

[4] S. Parikh, *et al.*, "A 32Gb/s Wireline Receiver with a Low-Frequency Equalizer, CTLE and 2-Tap DFE in 28nm CMOS", *ISSCC Dig. Tech. Papers*, pp. 28-29, Feb. 2013.

[5] H. Kimura, *et al.*, "28Gb/s 560mW Multi-Standard SerDes with Single-Stage Analog Front-End and 14-Tap Decision Feedback Equalizer in 28nm CMOS", *ISSCC Dig. Tech. Papers*, pp. 38-39, Feb. 2014.

 978-1-4799-6224-2/15/$31.00

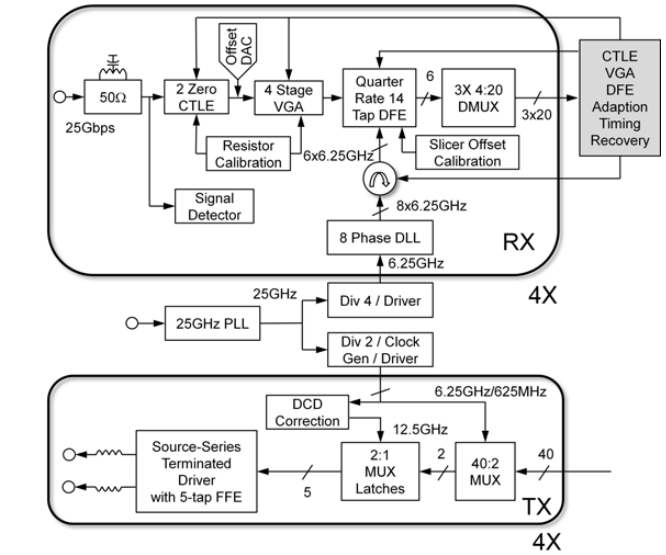

Figure 3.1.1: Block diagram of the transceiver.

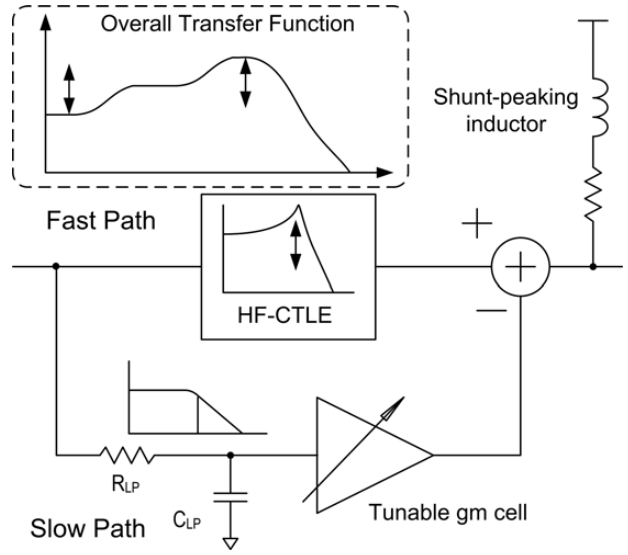

Figure 3.1.2: Programmable two-zero continuous-time linear equalizer.

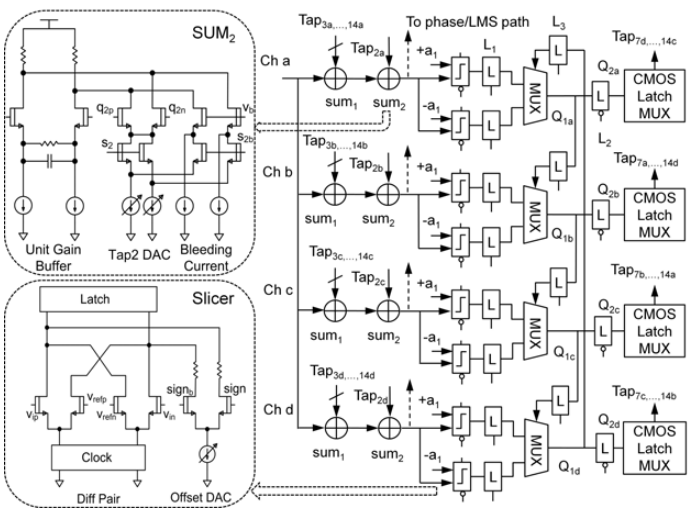

Figure 3.1.3: Block diagram of 14-tap DFE data path and schematics of summer 2 and reference-based slicer with offset calibration DAC.

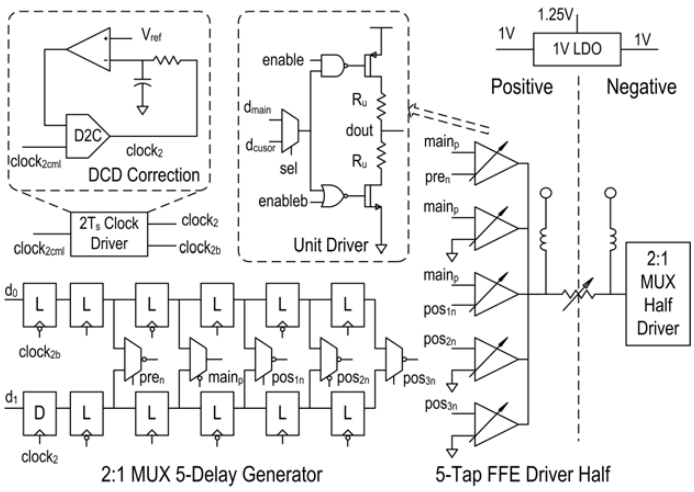

Figure 3.1.4: 5-tap FFE SST driver implementation with 2:1 MUX.

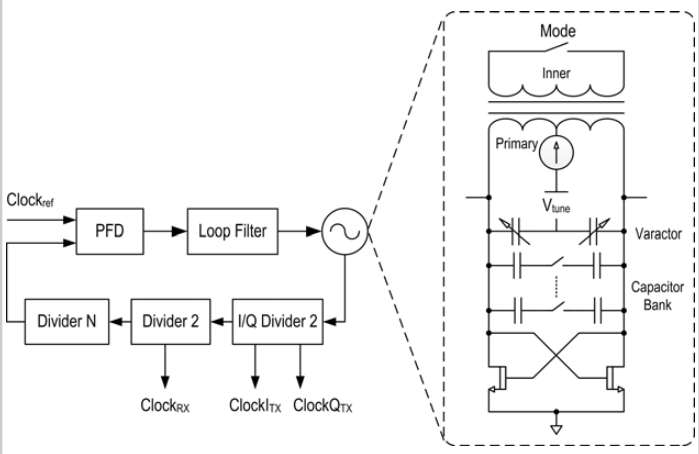

Figure 3.1.5: PLL block diagram with transformer-based LC-VCO.

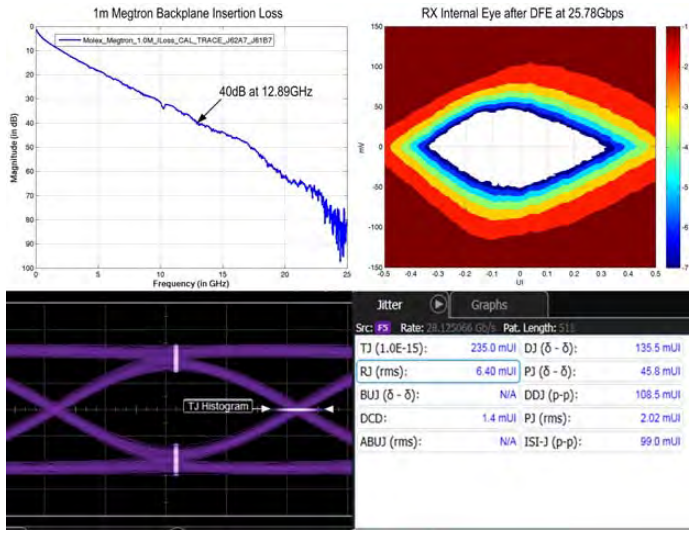

Figure 3.1.6: 40dB backplane insertion loss and RX internal eye at 25.78Gb/s (upper) and 28.125Gb/s TX eye diagram (bottom).

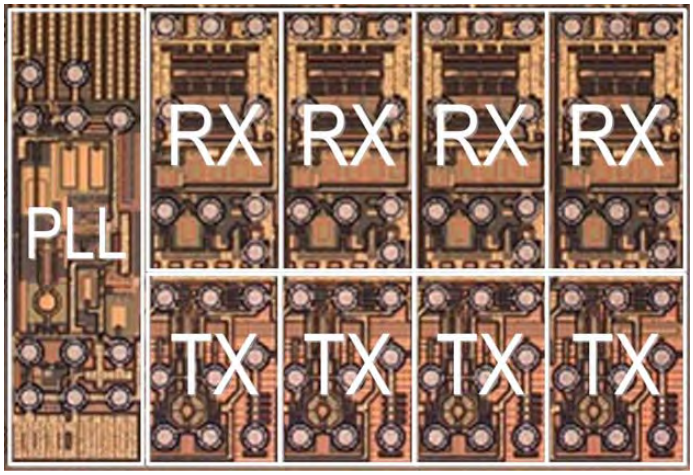

Figure 3.1.7: Die micrograph of four transceivers with a common PLL.

978-1-4799-6224-2/15/$31.00