27.9 A 200kS/s 13.5b Integrated-Fluxgate Differential-Magnetic-to-Digital Converter with an Oversampling Compensation Loop for Contactless Current Sensing

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High voltage applications such as electric motor controllers, solar panel power inverters, electric vehicle battery chargers, uninterrupted and switching mode power supplies benefit from the galvanic isolation of contactless current sensors (CCS) [1]. These include magnetic sensors that sense the magnetic field emanating from a current-carrying conductor. The offset and resolution of Hall-effect sensors is in the µT-level [1-3], in contrast to the nT-level accuracy of integrated-fluxgate (IFG) magnetometers [4]. Previously reported sampled-data closed-loop IFG readouts have limited BWs as their sampling frequencies (f_S) are limited to be less than or equal to the IFG excitation frequency, f_{EXC} [5-7]. This paper describes a differential closed-loop IFG CCS with $f_S > f_{EXC}$. The differential architecture rejects magnetic stray fields and achieves 750× larger BW than the prior closed-loop IFG readouts [6-7] with 10× better offset than the Hall-effect sensors [1-3].

The IFG sensors in this work are made by back-end processing on top of CMOS wafers. Each IFG has two magnetic cores sandwiched between excitation, sense and compensation coils, L_{comp}, made by two-layer metal windings. The IFG is sensitive to fields in parallel with the die, and so the CCS has two aligned IFGs on top of a U-shaped PCB trace carrying current I_{meas} (Fig. 27.9.1). I_{meas} produces differential magnetic terms B_{DM} along the two IFGs in contrast to stray-field B_{CM}. To avoid their transfer curve non-linearity, the IFGs are operated in feedback magnetic compensation loops (MCL) for near-zero internal field operation [6]. A precision differential MCL, MCL_{DIFF}, integrates the difference of the two IFG V_{demod} voltages and drives a fully balanced current into their L_{comp} coils to null B_{DM} terms in their cores (Fig. 27.9.1). A coarse common-mode MCL, MCL_{CM}, integrates the sum of their V_{demod} voltages to null B_{CM}. The MCL_{DIFF} integrator produces the CCS output signal. The CCS full-scale I_{meas} is mapped to the MCL_{DIFF} full-scale range of B_{DM} at the application level by geometrical scaling of the current carrying conductor and the spacing between the conductor and the IFGs. This enables the adaptation of the CCS to a wide range of applications.

Previously reported sampled-data closed-loop IFG readouts form first-order [5] or second-order MASH [6] magnetic-domain ΔΣMs or embed a SC-ΔΣM in the sense-path of an MCL with a digital loop filter and an FIRDAC (FIR filter combined with a DAC) in the feedback [7]. A challenge with embedding oversampled data-conversion into an IFG MCL is extending the readout BW independently of f_{EXC}. Direct oversampling of V_{demod} results in large f_S values if no anti-aliasing is used in the sense path. Furthermore, the compensation path only affects the sense signal during the transitions of the excitation signal. Since an IFG does not provide filtering in the magnetic-domain, oversampled compensation signals need to be band-limited.

The forward path of the proposed MCL_{DIFF} for the CCS (Fig. 27.9.2) includes a CTΔΣM followed by a digital loop filter (DLF). The DLF integrates the loop error signal, limits its noise BW, filters the CTΔΣM bitstream and provides notches at f_{demod} harmonics. The DLF output drives the feedback path that involves a single-bit digital ΔΣM (DΔΣM) and an FIRDAC, whose fully balanced output current through the L_{comp} coils results in the average differential V_{demod}, sensed by the forward path, converging to zero. An output $SINC_1$ filter decimates the DLF output to D_{out} at the data rate of f_{DR}.

The CTΔΣM processes the MCL error signal (residual B_{DM} in the cores) and its CT loop filter anti-alias filters the V_{demod} difference, enabling the use of $f_S > f_{EXC}$. The analog gain A before it (Fig. 27.9.2) reduces its IFG-referred quantization noise, enabling the use of multi-bit quantization with no need for DEM or DWA. With A=30dB, an 11b CTΔΣM is sufficient for >15b (quantization-noise-limited) CCS resolution.

The FIRDAC frequency response is designed to filter the DΔΣM truncation noise and provide notches at the harmonics of f_{EXC}, which prevents noise folding through the IFG demodulators. The use of a single-bit, fully balanced current-domain FIRDAC guarantees linearity and offset-free operation as component mismatch results in frequency response variation only.

The symmetrical impulse-response of the FIRDAC allows the implementation of only half of the current sources by folding its shift-register (Fig. 27.9.2). The compensation current affects MCL only during the IFG excitation transitions, when the magnetic cores are driven in and out of saturation (magnetic sampling). A digital S/H, consisting of a row of latches between the shift-register and the current sources, synchronizes the FIRDAC output to the IFG magnetic core saturation at $2f_{EXC}$. This has no noise folding penalties, as the FIRDAC suppresses noise at f_{EXC} harmonics, but offers two advantages. First, with saturated cores, the L_{comp} inductance drops from µH to nH levels, simplifying the FIRDAC current switching due to the smaller inductive load. Secondly, the FIRDAC jitter requirement is relaxed to a quarter of the f_{EXC} period.

The detailed CCS block diagram (Fig. 27.9.3) shows both the MCL_{DIFF} and MCL_{CM} loops. The forward and feedback paths of MCL_{DIFF} are sampled at f_S=10MHz and $2f_S$, respectively. The second-order CTΔΣM front-end contains two gain-boosted transconductors, $gm_{DM1,2}$, with embedded demodulators operating at f_{demod}=2MHz. The difference of their output currents is integrated by the first integrator of the CTΔΣM, whose quantizer and feedback DACs resolve 15-levels. A 30dB ratio between $gm_{DM1,2}$ and the CTΔΣM feedback coefficient sets the analog gain A (Fig. 27.9.2). The residual offset due to the charge injection of the demodulator switches is chopped at $f_{chop,DM}$=200kHz, whose artifacts are removed by the output $SINC_1$ filter decimating to f_{DR}=200kHz. The DLF is made by a digital integrator and a $SINC_2$ filter.

The single-bit third-order DΔΣM in the feedback path drives the FIRDAC. With 58 coefficients, the FIR filter has a third-order sinc response (Fig. 27.9.3). This is realized by 29 gain-boosted floating current sources running through both L_{comp} coils, whose shared terminals are biased at a DC voltage. The loop stability is determined by a digital gain-factor K_{dig}. The MCL_{CM} analog loop adds and integrates the demodulated IFG sense signals through $gm_{CM1,2}$ and drives a pair of matched push/pull current drivers commuted at $f_{chop,CM}$=200kHz.

The CCS (Fig. 27.9.7) is fabricated in a 0.6µm CMOS technology. The chip has an area of 9.8mm^2 and consumes 56mA from a 5V supply. For flexibility, the DLF, $SINC_1$ and DΔΣM were realized in an FPGA. A 1cm-wide current-carrying U-shaped PCB trace runs under the chip and has a B_{DM}/I_{meas} sensitivity of 26µT/A at the IFG positions (approximately 1.5mm above the PCB top layer). The FIRDAC full-scale current of ±12mA corresponds to -3.5dBFS stable range of ±1.328mT (B_{DM}) and an I_{meas} of ±51.07A with the showcased PCB configuration. The trace-width and vertical displacement to the die determine the current to B_{DM} translation gain, enabling the application-level scaling factor. The ±50A dynamic range, which is enabled by this specific PCB-level configuration, fits applications such as motor controllers or power inverters; however, the range can be extended significantly by the use of other primary conductors such as scaled bus-bars. Without using a zero-Gauss chamber, the raw transfer characteristic of 5 devices was measured from -5 to 5A (Fig. 27.9.4). A max offset of 35.4mA (900nT or 3LSBs) and uncalibrated gain deviation of ±1% (rms) is observed. A linear-fit shows a max non-linearity of ±5mA (±0.1%) over this range. With K_{dig}=43dB, the small and large-signal step responses show loop stability (Fig. 27.9.5). At a measured small-signal closed-loop BW of 75kHz its input-referred rms noise is 8.18mA (212nT rms) corresponding to an ENOB of 13.5. For a $100mA_{pk-pk}$ I_{meas} at 10kHz, the measured output spectra of the CTΔΣM, DΔΣM and the decimated output as well as a comparison to the state-of-the-art integrated magnetometers are shown in Fig. 27.9.6.

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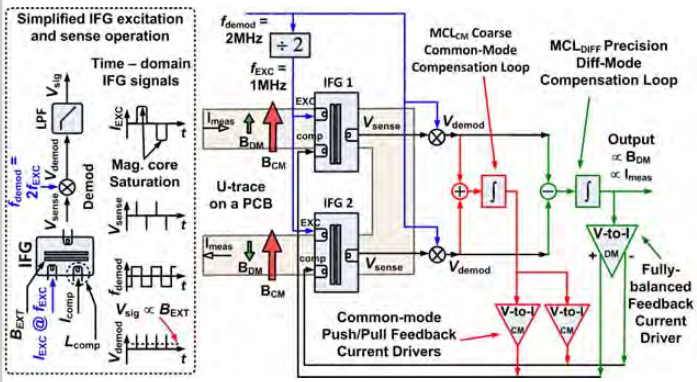


Figure 27.9.1: Simplified diagram of an IFG and its time-domain excitation and sense signals (left) and the differential CCS with MCL_{DIFF} and MCL_{CM} with the top-view of the PCB U-shaped trace and the orientation of two IFGs (right).

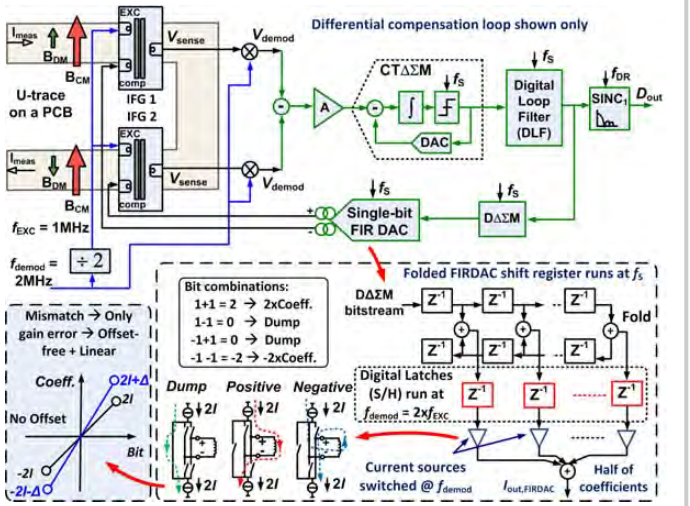


Figure 27.9.2: Simplified block diagram of the sampled-data MCL_{DIFF} (top) and simplified block diagram of the fully balanced folded FIRDAC (bottom-right) and the operation of its current sources (bottom-left).

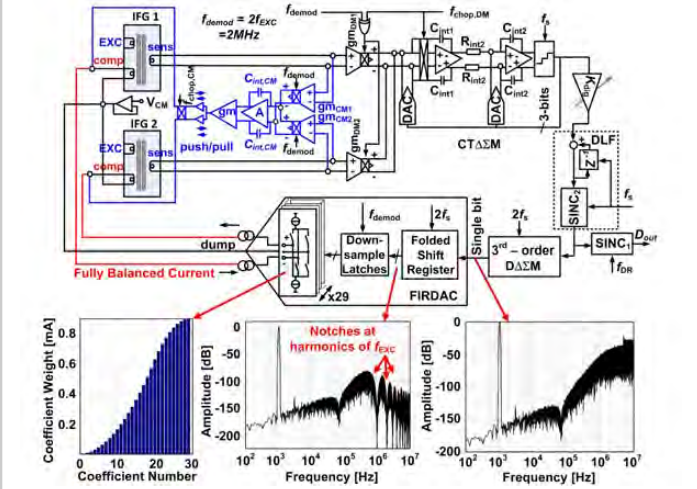
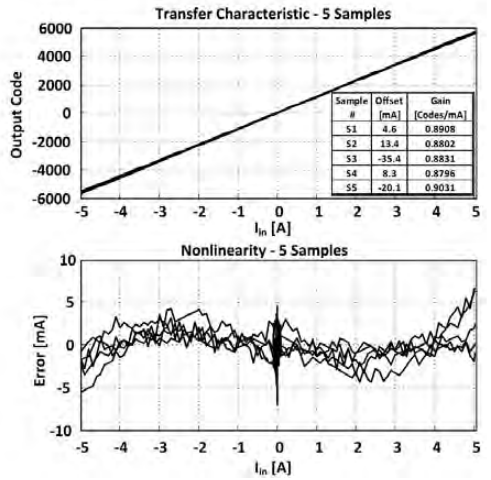


Figure 27.9.3: Detailed block-diagram of the CCS with the analog common-mode and sampled-data differential-mode MCLs around the two IFGs (top) and the FIRDAC coefficients and simulated spectra of DΔΣM and FIR filter outputs (bottom).



Sample #	Offset [mA]	Gain [Codes/mA]
S1	4.6	0.8908
S2	13.4	0.8802
S3	-35.4	0.8831
S4	8.3	0.8796
S5	-20.1	0.9031

Figure 27.9.4: DC transfer characteristic of 5 samples characterized over an input current range from -5 to 5A, including the offset and gain value summaries (top) and the deviation of the characteristic of each sample from a linear fit (bottom).

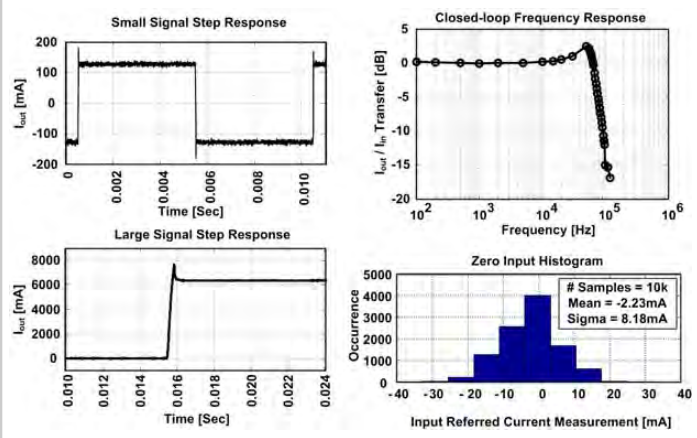
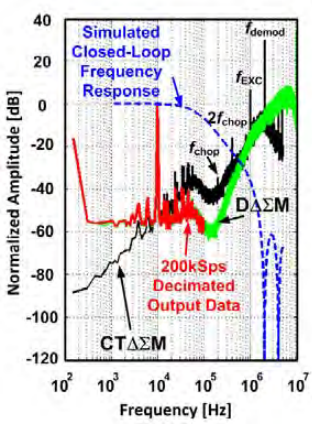


Figure 27.9.5: Small and large signal step-responses (left). Closed-loop MCL_{DIFF} frequency response (top-right), zero input histogram with offset and rms noise values (bottom-right).



Reference	This work	[5]	[6]	[7]	[3]
Sensor	IFG (Diff)	IFG	IFG	IFG	Hall
Tech. [µm]	0.6	0.8	0.35	0.35	0.35
Area [mm2]	9.8	19	20	9	6.4
I_supply [mA]	56	65	14.8	11	5
Range	±1.32 mT (diff)	±100 µT	±2 µT	±120 µT	±0.5 mT
BW	75kHz	NA	30Hz	100Hz	100Hz
Non-linearity	±0.1%	±1.5%	NA	NA	±0.5%
Offset	900nT (diff)	NA	NA	NA	10µT
Resolution	13.5 bits	NA	15 bits (92dB)	13 bits (3.4nT/√Hz)	12 bits

NA = Not available

Figure 27.9.6: Normalized spectra of measured CTΔΣM & DΔΣM and the 200kSps decimated output (65536-point 16×-avgerage Hann-window FFT) for 100mA peak-to-peak 10kHz input current and simulated closed-loop frequency response (left) and comparison to state-of-the-art magnetometers (right).

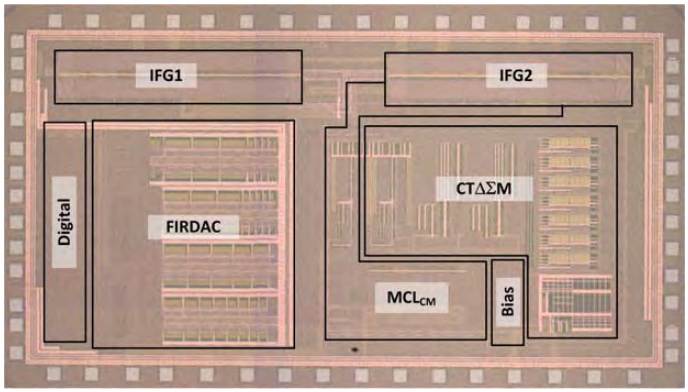


Figure 27.9.7: Chip micrograph of the CCS based on the differential integrated-fluxgate magnetic-to-digital converter.

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1

1P1M 1-Polysilicon layer 1-Metal layer
1T1C 1-Transistor 1-Capacitor

3

3D 3-Dimensional
3G Third-Generation (Wireless)
3T 3-Transistor

6

6T 6-Transistor

8

8T 8-Transistor

ΔΣ

ΔΣ Delta-Sigma
ΔΣM Delta-Sigma Modulator

ΣΔ

ΣΔ ΔΣ is preferred.
ΣΔM ΔΣM is preferred.

A

a-Si Amorphous Silicon
AC Alternating Current
A/D Analog-to-Digital Converter
AAC Advanced Audio Coding
ACI Adjacent-Channel Interface
ACL Access Control List
ACLR Adjacent-Channel Leakage Power Ratio
ACPR Adjacent-Channel Power Ratio
ADC Analog-to-Digital Converter
ADDLL All-Digital DLL
ADPLL All-Digital PLL
ADSL Asynchronous Digital Subscriber line
ADU Analog-to-Digital Unit
AES Advanced Encryption Standard
AFC Automatic Frequency Control
AFE Analog Front End
AFM Adaptive Flash Management ™
AGC Automatic Gain Control
AGU Address-Generation Unit
AIP Artificial-Intelligent Partner
ALU Arithmetic Logic Unit
AM Amplitude Modulation
AMI Advanced Metering Infrastructures
AMLCD Active-Matrix LCD
AMOLED Active-Matrix OLED
AMP Asymmetric Multi-Processing
AMPS Advanced Mobile-Phone Service
AMS Analog Mixed-Signal {System}
APD Avalanche Photo-Diode
APG Algorithmic Pattern Generator
API Application-Programming Interface
APSK Amplitude Phase-Shift Keying
ARM Advanced RISC Machine
ASIC Application-Specific Integrated Circuit
ASK Amplitude Shift Keying
ASP Average Selling Price
ASP Advanced Simple Profile {MPEG-4 Video}
ATA Advanced Technology Attachment
ATD Address-Transition Detection
ATE Automatic Test Equipment
ATM Asynchronous Transfer Mode
ATSC Advanced Television Systems Committee
AVC Audio-Visual CODEC
AVC Automatic Volume Control {use AGC}
AWG Arrayed-Waveguide Grating

B

BAN Business Area Network
BAW Bulk Acoustic Wave
BB Baseband
BBT Band-to-Band Tunneling
BCD Bipolar-CMOS-DMOS Process
BCD Binary-Coded Decimal
BCH Bose-Chaudhuri-Hocquenghem {a type of error-correcting code}
BD Blu-ray disc
BER Bit-Error Rate
BGA Ball-Grid Array
BGR Band-Gap Reference
BiCMOS Bipolar Complementary-MOS
BIOS Basic Input/Output System
BIST Built-in Self-Test
BJT Bipolar Junction Transistor
BL Bitline
BLE Bluetooth Low Energy
BOM Bill of Materials
BPF Bandpass Filter
BPSK Binary Phase-Shift Keying
BSI BackSide Illumination
B-VOP Bidirectional-Video Object Planes
BW Bandwidth

C

C4 Controlled-Collapse Chip Connection
CAD Computer-Aided Design
CAM Content-Addressable Memory
CAN Controller Area Network
CAS Column-Address Strobe
CCCS Current-Controlled Current Source
CCD Charge-coupled Device
CCK Complementary Code Keying
CCO Current-Controlled Oscillator
CCVS Current-Controlled Voltage Source
CDAC Capacitor DAC
CDMA Code-Division Multiple Access
CDR Clock and Data Recovery
CDS Correlated Double Sampling
CF Compact Flash
CFA Color Filter Array
CFL Compact Fluorescent Lamp
CHE Channel Hot-Electron (Injection)
CIS Complex-Instruction-Set Computer
CIS CMOS Image Sensor
CLI Command Line Interface
CML Current-Mode Logic
CMOS Complementary Metal-Oxide Semiconductor
CMRR Common-Mode Rejection Ratio
CMU Clock Multiplier Unit
CMUT: Capacitive micromachined ultrasonic transducer
CNFET Carbon Nanotube NFET
CO Central-Office {hardware}
CODEC Coder-Decoder
COFDM Coded FDM
CoMP Coordinated MultiPoint
CPE Customer Premises Equipment
CPU Central Processing Unit
CPW CoPlanar Waveguide
CRC Cyclic Redundancy Check
CSMA Carrier-Sense Multiple Access
CT Continuous Time {system}
CUI Command User Interface
CVD Chemical Vapor Deposition

D

D/A Digital-to-Analog Converter
DAB Digital-Audio Broadcasting
DAC Digital-to-Analog Converter
dBFS dB relative to Full Scale
DBS Direct-Broadcast Satellite
DCC Duty-Cycle Corrector
DCO Digitally Controlled Oscillator
DCT Discrete Cosine Transform
DCVS Differential Cascode Voltage Switch
DCVS Digitally-Controlled Voltage Source
DCXO Digitally Controlled Crystal Oscillator
DDFS Direct-Digital Frequency Synthesis (or synthesizer)
DDR Dual Data Rate
DDS Direct Digital Synthesis
DECT Digitally Enhanced Cordless Communication
DEM DEModulator
DEM Dynamic Element Matching
DEMOS Depletion MOS
DEMUX Demultiplexer
DES Data-Encryption Standard
DEVM Differential Error Vector Magnitude
DFE Decision-Feedback Equalizer
DFF D-type Flip Flop
DFT Design for Testability
DFT Discrete Fourier Transform
DfY Design-for-Yield
DIMM Dual In-Line Memory Module
DIP Dual In-line Package
DLL Delay-Locked Loop
DMA Direct Memory Access
DMB Digital Multimedia Broadcasting
DMIPS Dhrystone Million Instructions Per Second
DMOS (Double-)Diffused MOS
DNA Deoxyribonucleic Acid
DNL Differential Non-Linearity
DNR Dynamic Range (DR preferred)
DPT Double Patterning Technology
DOM Digital Optical Module
DR Dynamic Range (see also DNR)
DRAM Dynamic Random-Access Memory
DRC Design-Rule Check
DSB Double Side Band
DSC Digital Still Camera
DSL Digital Subscriber Line
DS-OFDM Direct-Sequence Orthogonal Frequency Division Multiplexing
DSP Digital Signal Processing
DSSS Direct-Sequence Spread-Spectrum
DT Discrete Time
DTL Diode-Transistor Logic
DTV Digital Television
DUT Device Under Test
DVB Digital-Video Broadcasting
DVB-C Digital-Video Broadcasting - Cable
DVB-H Digital-Video Broadcasting - Handhelds
DVB-S Digital-Video Broadcasting - Satellite
DVB-T Digital-Video Broadcasting - Terrestrial
DVD Digital Video Disc
DVFS Dynamic Voltage Frequency Scaling
DVS Dynamic Voltage Scaling
DWA Data Weighted Averaging
DWDM Dense-Wavelength-Division Multiplexing
DWMT Discrete Wavelet Multi-Tone

E

ECC Error-Correcting Code
ECG Electro-CardioGram
ECL Emitter-Coupled Logic
ECP Emitter-Coupled Pair
EDGE Enhanced Data rates for Global Evolution
EDR Enhanced Data Rate
EEG Electro-EncephaloGram
EEPROM Electrically Erasable Programmable Read-Only Memory
EFR Enhanced Full-Rate {GSM}
EIRP Effective Isotropic Radiated Power
EKG Electro-CardioGram (see ECG)
EMG ElectroMyoGram
EMI Electro Magnetic Interference
eICIC enhancement in Inter-Cell Interference Coordination
ENOB Effective Number of Bits
EOT Electrical Oxide Thickness
EPON Ethernet-based Passive Optical Network
EPROM Erasable Programmable Read-Only Memory
ERBW Effective-Resolution Bandwidth
ESD ElectroStatic Discharge
EUV Extreme UltraViolet
EVDO EVolution Data Optimized (in the context of CDMA)
EVM Error-Vector Magnitude
EWC Enhanced Wireless Consortium

F

f_{max} Unity power gain frequency.
f_s Sampling frequency
f_t Transit frequency
FAMOS Floating-gate Avalanche-injection MOS Transistor
FAN Field Area Network
FBAR Film Bulk Acoustic Resonator
FBDIMM Fully Buffered DIMM
FCC Federal Communications Commission (U.S.)
FDM Frequency-Division Multiplexing
FDMA Frequency-Division Multiple-Access
FDNR Frequency-Dependent Negative Resistor
FDSOI Fully Depleted Silicon-on-Insulator
FEC Forward Error Checking
FEM Front End Module
FeRAM Ferro-electric Random Access Memory
FET Field-Effect Transistor
FF Flip-Flop
FFC Flexible-Flat Cable
FFE Feed-Forward Equalizer
FFT Fast Fourier Transform
FIB Focused Ion Beam
FIFO First In-First Out
FinFET A MOSFET with the gate on two sides {acronym describes the physical shape}
FIR Finite Impulse Response {filter}
FLOPS Floating-Point Operations Per Second
FLOTOX Floating-gate Tunnel OXide
FM Frequency Modulation
FMCW Frequency Modulated Continuous Wave
FN Fowler-Nordheim
FO4 Fan-Out of 4
FOM Figure Of Merit
FPGA Field-Programmable Gate Array
FPN Fixed Pattern Noise
FPU Floating Point Unit
FSG FluoroSilicate glass {dielectric}
FSG Fluorine-doped Silicate Glass
FSK Frequency-Shift Keying
FSM Finite-State Machine

G

GAA	Gate-All-Around
GaN	Gallium Nitride
GBW	Gain-BandWidth {product}
GCA	Gain-Controlled Amplifier
GDDR	Graphics Double-Data-Rate
GDfM	Generalized Design-for-Manufacturability
GE-PHY	Gigabit-Ethernet Physical
GFSK	Gaussian Frequency-Shift Keying
GFLOPS	Giga Floating-Point Operations Per Second
GIDL	Gate-Induced Drain Leakage
GMSK	Gaussian Minimum-Shift Keying
GOPS	Giga-Operations Per Second
GPRS	General Packet-Radio Service
GPS	Global Positioning System
GPU	Graphic Processing Unit
GSM	Global Standard for Mobile Communication
GUI	Graphical User Interface
GVCO	Gated VCO

H

HBT	Hetero-junction Bipolar Transistor
HBM	High-Bandwidth Memory
HBM	Human Body Model
HCI	Host-Controller Interface
HCI	Human-to-Computer Interface
HD	High-Density
HDD	Hard-Disk-Drive
HDL	Hardware-Description Language
HDTV	High-Definition TeleVision
HD2	2nd order Harmonic Distortion
HD3	3rd order Harmonic Distortion
HiFi	High Fidelity
Hk	High-k dielectric
HMD	Head Mounted Display
HPF	High-Pass Filter
HSPDA	High-Speed Downlink Packet Access
HT3	Hypertransport 3 (I/O standard)
HTM	Hierarchical Temporal Memory
HV	High Voltage
HVAC	Heating, Ventilation and Air Conditioning
HVCMOS	High-Voltage Complementary MOS
HVMOS	High-Voltage MOS

I

I/O	Input-Output
I/Q	In Phase and Quadrature
IAN	Industrial Area Network
IBOC	In-Band Out-of-Channel
IC	Integrated Circuit
ID	Identification
IF	Intermediate Frequency
IGBT	Insulated Gate Bipolar Transistor
IIP2	Input-referred Input 2nd-order Intercept Point
IIP3	Input-referred Input 3rd-order Intercept Point
IIR	Infinite Impulse Response Filter
IMD	Inter-Modulation Distortion
IM2	2nd-order InterModulation distortion
IM3	3rd-order InterModulation distortion
INL	Integral Non-Linearity
InP	Indium Phosphide
IoT	Internet of Things
IP	Intellectual Property
IPC	Inter-Process Communication
IPSEC	Internet (Network) Protocol for Security
IR	Image Rejection
IR	InfraRed
ISDB	Integrated Services Digital Broadcasting
ISDB-C	Integrated Services Digital Broadcasting - Cable
ISDB-S	Integrated Services Digital Broadcasting - Satellite
ISDB-T	Integrated Services Digital Broadcasting - Terrestrial
ISFET	Ion-Sensitive Field-Effect Transistor
ISI	Inter-Symbol Interference
ISM	Industrial, Scientific and Medicine Band
ITU-T	International Telecommunications Union

J

JPEG	Joint Photographic Expert Group
JTAG	Joint Test-Automation Group

K

KGD	Known Good Die

L

LAGS	Locally-Asynchronous Globally-Synchronous
LAN	Local-Area Network
LBS	Location-Based Services
LCD	Liquid-Crystal Display
LCOS	Liquid-Crystal On Silicon
LDI	LVDS Display Interface
LDCMOS	Laterally Diffused Complementary Metal-Oxide Silicon
LDMOS	Laterally Diffused Metal-Oxide Silicon
LDO	Low Drop-Out {regulator}
LDPC	Low-Density Parity Check
LED	Light-Emitting Diode
LEP	Light-Emitting Polymer
LFCSP	LeadFrame Chip-Scale Package
LFSR	Linear-Feedback Shift Register
LHC	Large Hadron Collider
LIN	Local Interconnect Network
LMS	Least Mean Square
LNA	Low-Noise Amplifier
LNB	Low-Noise Blockers
LO	Local Oscillator
LPCVD	Low-Pressure Chemical-Vapor Deposition
LPF	Low-Pass Filter
LRU	Least-Recently Used
LSB	Least-Significant Bit
LSI	Large-Scale Integration
LTE	Long Term Evolution
LTPS	Low-Temperature-Poly Silicon
LV	Low Voltage
LVDS	Low-Voltage Differential Signaling
LVS	Layout Verification to Schematic

M

MAC	Media-Access Controller
MAC	Mutiply-Accumulate
MASH	Multi-stAge noise SHaping
MBOA	Multi-Band OFDM Alliance
MB-OFDM	Multi-Band OFDM
MCM	Multi-Chip Module
MCP	Multi-Chip Package
MCU	MicroController Unit
MCU	Multipoint Conferencing Unit
MDAC	Multiplying DAC
MEMS	Micro-Electro-Mechanical System
MER	Modulation Error Ratio
MfD	Manufacturing-for-Design
MPU	Microprocessor Units
microSD	micro Secure Digital
MICS	Medical Implant Communication Band
MIM	Metal-Insulator-Metal
MIMO	Multiple- Input, Multiple-Output
MIPI	Mobile Industry Processor Interface
MIPS	Million Instructions Per Second
MISR	Multiple-Input Signature Register
ML	Matchline

MLC Multi-Level Cell
MLSD Maximum-Likelihood-Sequence Detection
MLSE Maximum-Likelihood-Sequence Estimation
MMAC Mega Mutliply-Accumulate
MMIC Monolithic Microwave Integrated Circuit
MMIO Memory-Mapped I/O
mmW millimeter-Wave
MODEM Modulator-Demodulator
MOS Metal-Oxide-Semiconductor (Silicon)
MOSFET Metal Oxide Semiconductor Field-Effect Transistor
MOST MOS Transistor
MOST Media-Oriented Systems Transport
MP Multi-Processor
MP3 MPeg-1 audio layer 3 (lossy compression algorithm)
MPEG Motion-Picture Expert Group
Mpps Million packets per second {VoIP}
MPPT Maximum-Power-Point Tracker
MPU Microprocessors
MSB Most Significant Bit
MRAM Magnetic Random-Access Memory
MRAM Magnetoresistive Random-Access Memory
MRC Maximum-Ratio Combining
MSB Most-Significant Bit
MTJ Magnetic Tunnel Junction
MTPR Multi-Tone Power Ratio
MUX Multiplexer
MWPC Multi-Wire Proportional Chamber

N

NAICS Network Assisted Interference Cancellation and Suppression
NAN Neighbourhood Area Network
NBTI Negative-Bias Temperature Instability
NEF Noise Efficiency Factor
NEM Nano-Electro-Mechanical system
NF Noise Figure
NFV Network Function Virtualization
NMOS N-channel MOS
NMOST NMOS Transistor
NoC Network on (a) Chip
NPN N-type-P-type-N-type bipolar (transistor)
NRTZ Non Return-To-Zero (see also NRZ)
NRZ Non-Retun- to-Zero (see also NRTZ)
NTF Noise Transfer Function
NVM Non-Volatile Memory
NVRAM Non-Volatile Random-Access Memory

O

ODT On-die Termination
OEM Original-Equipment Manufacturer
OFDM Orthogonal Frequency-Division Multiplexing
OIF Optical-Internetworking Forum
OIP2 Output-referred intercept point for 2nd-order distortion
OIP3 Output-referred intercept point for 3rd-order distortion
OLED Organic LED
ONO Oxide-Nitride-Oxide
OOK On-Off Keying
OSR Over-Sampling Ratio
OTA Operational Transconductance Amplifier
OTP One Time Programmable

P

P_{1dB} 1dB gain-compression Point
PA Power Amplifier
PA Public-Address {system}
PAE Power-Added Efficiency
PAM Pulse-Amplitude Modulation
PAN Personal-Area Network
PCB Printed-Circuit Board
PCH Platform Controller Hub
PCI Peripheral-Component Interconnect
PCI-X PCI Express
PCM Pulse-Code Modulation
PCS Personal Communication Services
PCU Power-management Control Unit
PD Phase Detector
PD-SOI Partially-Depleted SOI
PDA Personal Data Assistant
PDN Power-Delivery Network
PDP Power-Delay Product
PFD Phase and Frequency Detector
PGA Programmable-Gain Amplifier
PGA Programmable Gate Array
PHEMT Pseudomorphic High-Electron-Mobility Transistor
PHEVs Plug-in Hybrid Electric Vehicles
PHY PHYsical layer {of a communications protocol}
PID Proportional, Integral, Derivative (a type of control loop)
PLA Programmable Logic Array
PLC Power-Line Communication
PLD Programmable Logic Device
PLL Phase-Locked Loop
PMOS P-channel MOS
PMOST PMOS transistor
PMU Power Management Unit
PNP P-type-N-type-P-type bipolar (transistor)
PON Passive Optical Network
PoP Package-on-Package
POTS Plain-Old Telephone Service
ppm parts per million
PPM Pulse-Position Modulation
PR Pseudo Random
PR Partial Response
PRAM Phase-Change RAM
PRBS Psuedo-Random Binary Sequence
PRML Partial-Response, Maximum-Likelihood
PROM Programmable Read-Only Memory
PSD Power Spectral Density
PSK Phase-Shift Keying
PSNR Peak SNR
PSRR Power-Supply Rejection Ratio
PTAT Proportional To Absolute Temperature
PV PhotoVoltaics
PVD Physical Vapor Deposition
PVT Process, Voltage, Temperature
PWM Pulse-Width Modulation

Q

QPT Quadruple Patterning Technology
QAM Quadrature Amplitude Modulation
QDR Quad Data Rate
QoS Quality of Service
QPSK Quadrature Phase-Shift Keying
QVCO Quadrature Voltage-Controlled Oscillator
QVGA Quarter Video Graphics Array

R

R/W ReadWrite
RAM Random-Access Memory
RAT Radio Access Technologies
RBW Resolution BandWidth
RDAC Resistor DAC
RDF Random Dopant Fluctuation
RF Radio Frequency
RFID RF ID (tag)
RISC Reduced-Instruction-Set Computer
ROM Read-Only Memory
rms root mean square

ROM	Read-Only Memory
RSA	A public-key cryptographic system, named after: Ron Rivest, Adi Shamir, and Leonard Adleman
RSSI	Received-Signal-Strength Indicator
RTL	Resistor-Transistor Logic
RTS	Random Telegraph Signal
RTZ	Return-To-Zero
RX	Receiver
RZ	Return-to-Zero (see also RTZ)

S

SAL	Service Abstraction Layer
SAR	Successive-Approximation-Register
SAW	Surface Acoustic Wave
SATA	Serial Advanced-Technology Attachment
SC	Switched-Capacitor
SCL	Source-Coupled Logic
SCP	Source-Coupled Pair
SCR	Silicon Controlled Rectifier
S-DMB	Satellite Digital-Multimedia Broadcasting
SD	Secure Digital (package type)
SDI	Software-Defined Infrastructure
SDN	Software-Defined Networking
SDR	Software Defined Radio
SDRAM	Synchronous Dynamic Random-Access Memory
SEM	Scanning Electron Microscope
SER	Soft-Error Rate
SER	Symbol-Error Rate
SerDes	Serializer/Deserializer
SFDR	Spurious-Free Dynamic Range
SFI	Serdes Framer Interface
SFP	Small Form-factor Pluggable
S/H	Sample-and-Hold
SHA	Sample-and-Hold Amplifier
SiC	Silicon Carbide
SiGe	Silicon Germanium
SiGe:C	Silicon, Germanium, Carbon
SIL	Safety Integrity Level
SILC	Stress-Induced Leakage Current
SIMD	Single-Instruction Multiple-Data
SINAD	SIgnal-to-Noise And Distortion (ratio)
SIO	Synchronous I/O
SIP	Single-Inline Package
SiP	System in (a) Package
SL	Searchline
SMP	Symmetric Multi-Processing
SMS	Short-Messaging Service
SNDR	Signal-to-Noise and Distortion Ratio
SNM	Static Noise Margin
SNR	Signal-to-Noise Ratio
SNS	Social-Network Service
SoC	System on (a) Chip
SOI	Semiconductor on Insulator
SONET	Synchronous Optical NETwork
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
SOS	Silicon On Saphire
SP	Simple Profile
SPAD	Single-Photon Avalanche Diode
SPDT	Single Pole Double Throw
SPI	System Packet Interface
SRAM	Static Random-Access Memory
SSB	Single Side-Band
SSC	Spread Spectrum Clocking
SSCG	Spread Spectrum Clock Generator
SSD	Sold State Disk
SSN	Simultaneous Switching Noise
SSO	Simultaneous Switching Output
SSTL	Stub Series Terminated Logic
SXGA	Super Extended Graphics Array

T

TC	Temperature Coefficient
TCAM	Ternary Content-Addressable Memory
TCON	Timing Controller
TCP	Transmission Control Protocol
TDC	Time-to-Digital Converter
TDDB	Time-Dependent Dielectric Breakdown
TDM	Time-Division Multiplexing
TDMA	Time-Division Multiple-Access
TD-SCDMA	Time-Division Synchronous Code-Division Multiple Access
TEM	Tunneling-Electron Microscope
TFLOPS	Tera Floating-Point Operations Per Second
TFT	Thin-Film Transistor
TIA	TransImpedance Amplifier
T/H	Track and Hold
THA	Track-and-Hold Amplifier
THD	Total Harmonic Distortion
THD+N	THD plus Noise
TLB	Translation Lookaside Buffer
ToF	Time of flight
TOPS	Tera-Operations Per Second
TSV	Through-Silicon Via
TTL	Transistor-Transistor Logic
TV	Television
TWh	Tera-Watt hour
TX	Transmitter

U

UD	Ultra-high Definition
UDTV	Ultra-high-Definition TeleVision
UGC	User-Generated Contents
UHDV	Ultra-High-Definition Video
UHF	Ultra-High Frequency
UI	Unit Interval
UI	User Interface
UIPP	UI_{pp} (peak-to-peak)
U-NII	Unlicensed National Information Infrastructure
UMPC	Ultra-Mobile-PC
UMTS	Universal Mobile-Telecommunication System
UPROM	Unerasable Programmable Read-Only Memory
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair
UWB	Ultra-WideBand
UXGA	Ultra-eXtended Graphics Array
UPF	Unified Power Format

V

V_t	MOS transistor threshold voltage
V_T	thermal voltage
VCCS	Voltage-Controlled Current Source
VCDL	Voltage-Controlled Delay Line
VCO	Voltage-Controlled Oscillator
VCVS	Voltage-Controlled Voltage-Source
VCXO	Voltage-Controlled Crystal Oscillator
VCSEL	Vertical-Cavity Surface-Emitting Laser
VDMOS	Vertically Diffused MOS
VDSL	Very high bit-rate Digital Subscriber Line
VGA	Variable-Gain Amplifier
VGA	Video Graphics Array
VLIW	Very Long Instruction Word
VLF	Very Low Frequency
VLSI	Very Large-Scale Integration
VoD	Vision on Demand
VoIP	Voice over IP
VR	Voltage Regulator
VRM	Voltage Regulator Module
VRT	Variable-Retention Time
VSB	Vestigial Side Band

VSoC	Virtual System-on-Chip
VSWR	Voltage Standing-Wave Ratio
VTG	Vertical-Transfer Gate

W

WAN	Wide-Area Network
WCDMA	Wideband Code-Division Multiple- Access
WDM	Wavelength-Division Multiplexing
WebRTC	Web Real-Time Communication
WEP	Wired-Equivalent Privacy
WiFi	Wireless Fidelity; {an interoperability certification for IEEE 802.11 WLAN products}
WiMax	Worldwide Interoperability for Microwave Access (IEEE802.16)
WL	Wordline
WLAN	Wireless Local-Area Network
WLCG	Worldwide LHC Computing Grid
WSN	Wireless Sensor Node

X

XAUI	(10 Gigabit) eXtended Attachment Unit Interface
XDR	Extreme Data Rate
XENPAK	10 Gb Ethernet-compatible fiber-optic standard
XFMR	TransForMeR
XFP	Small form-factor pluggable
XGA	Extended Graphics Array
XO	Crystal Oscillator

Z

ZB	Zettabyte

ISSCC 2015

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Timetable

T1: Fundamentals of Modern RF Receivers

To be compliant with multi-standard applications, the RF front-end of a modern transceiver must satisfy several challenging tasks such as large operative bandwidth, low noise, and high linearity. Over the years, addressing such requirements has significantly changed the radio architecture towards an ultimate solution based on current signal processing and passive mixers. In this tutorial, after a brief description of the typical structure of a receiver, the main properties that the radio must satisfy will be defined. After that, voltage and current signal processing will be compared showing why a fully current-mode approach is more suitable in deep-scale technologies. The tutorial will end by describing the most popular RF front-end architectures with a particular emphasis on the noise-canceling technique and the Class-AB solutions.

Instructor: Antonio Liscidini

Antonio Liscidini received the Laurea degree and Ph.D. in Electrical Engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006 respectively. He was a summer intern at National Semiconductor in 2003 (Santa Clara, CA) studying polyphase filters and CMOS LNAs. From 2008 to 2012 he was Assistant Professor at the University of Pavia and consultant for Marvell Semiconductor in the area of integrated circuit design. In December 2012 he joined the Edward S. Rogers Sr. Department of Electrical & Computer Engineering of the University of Toronto. His research interests are in the implementations of transceivers and frequency synthesizers for cellular and ultra-low-power applications.

T2: Basics of DRAM Interfaces

Memories have evolved continuously since the simple days of SDRAM. Back then, one interface standard was dominating and could be adapted to the different system needs. Now, one size no longer fits all. The number of DRAM standards is proliferating since different system environments require different, tailored DRAM-solutions. Examples are DDRn, GDDR5, HBM, LPDDRn, and WIOn. In this tutorial, we give an overview of these interface standards highlighting important details of the specifications, and describe selected design aspects and their system level implications.

Instructor: Martin Brox

Martin Brox received Dipl. and Dr. degrees from the University of Münster in 1988 and 1992. In 1988 he joined Siemens Corporate Research for a project to improve the modeling of hot-carrier degradation on CMOS-circuits. In 1992, he moved to the IBM/Siemens/Toshiba DRAM development alliance initially focusing on design, layout and test of DRAM mini-arrays and later DRAM-design. In 1997, he joined Siemens Semiconductor which later became Infineon and Qimonda where he was responsible for multiple commodity, RDRAM, GDDR3 and GDDR5 designs. In 2009 he joined Elpida (now part of Micron) as the lead design engineer for Micron's GDDR5 development.

T3: Ultra-Low-Power Wireless Systems

Emerging applications such as wearable devices, sensor networks and the 'internet of things' have to operate from very limited power budgets, and thus ultra-low-power operation is becoming increasingly important. This tutorial will address a range of issues that need to be considered in the design of ultra-low-power wireless systems. The tutorial will describe key features of low-power wireless standards such as BTSmart. We will then give an overview of architectures appropriate for very low power implementation including super-regenerative receivers, BAW-based architectures and direct modulation transmitters, and will outline the system trade-offs, which need to be considered for specific applications. We will then consider some key circuit building blocks required in the receiver, transmitter, and peripheral units and outline design techniques that are suitable for very low power implementation.

Instructor: Alison Burdett

Alison Burdett has over 25 years of experience in semiconductor design. She joined Toumaz in 2001 as Technical Director, and is currently responsible for delivering silicon and healthcare technology programs within the company. Prior to joining Toumaz, Alison spent time both in industry as an integrated circuit designer, and also in academia (as Senior Lecturer in Analogue IC Design at Imperial College London) Dr. Burdett is a Chartered Engineer, a Fellow of the Institute of Engineering and Technology (FIET) and a Senior Member of the IEEE. She is European Regional Chair of the Technical Program Committee for the IEEE International Solid State Circuits Conference (ISSCC), a member of the National Microelectronics Institute (NMI) Microelectronics Design Advisory Board, and a Visiting Researcher at the Institute of Biomedical Engineering, Imperial College.

T4: Low-Power Near-threshold Design

Digital circuit energy efficiencies plateaued due to stagnated voltage scaling in sub-90nm technologies. As a result, there is renewed interest in operating circuits at low supply voltages, such as near the device threshold voltage (referred to as near-threshold or NT design). NT operation offers a good balance between performance and energy efficiency, in contrast to sub-threshold design, which sacrifices performance for energy optimality. This tutorial offers design guidelines for near-threshold operation, particularly related to NT design robustness. Design examples from both academia and industry will highlight DSP accelerators, embedded memories, wide-range voltage scalable designs, and variability compensation strategies that scale to NT voltages.

Instructor: Dennis Sylvester

Dennis Sylvester received a Ph.D. from the University of California, Berkeley and is Professor of Electrical Engineering and Computer Science at the University of Michigan, Ann Arbor, MI. He has published over 375 articles along with one book and several book chapters, and holds 20 US patents. His research interests include the design of millimeter-scale computing systems and energy-efficient near-threshold computing. He is co-founder of Ambiq Micro, a fabless semiconductor company developing ultra-low-power mixed-signal solutions for compact wireless devices. He is an IEEE Fellow.

T5: High-Speed Current-Steering DACs

Among the various existing digital-to-analog converter (DAC) architectures, the current- steering DAC architecture prevails at high sampling rates. Its simple underlying topology makes these DACs well-suited for implementation in deep-submicron CMOS processes, where high-speed switches are readily available. The topological simplicity, however, comes with a substantial sensitivity to many sources of distortion. This tutorial first summarizes the basics of the current-steering architecture. Subsequently, it covers the various distortion mechanisms as well as the design techniques available to overcome their detrimental effects on DAC performance. Finally, measurement techniques required to assess the performance of the eventual DAC design are treated.

Instructor: Jan Mulder

Jan Mulder received the M.Sc. and Ph.D. degrees in electrical engineering from Delft University of Technology, The Netherlands, in 1994 and 1998, respectively. From 1998 to 2000, he was with Philips Research Laboratories, Eindhoven, The Netherlands. In 2000, he joined Broadcom, Bunnik, The Netherlands, where he has been involved in analog and mixed-signal IC design. He has published over 60 papers and holds more than 35 U.S. patents in circuit design. He served as an Associate Editor for IEEE Trans. on CAS-1 and is a member of the ISSCC ITPC.

T6: Clock and Data Recovery Architectures and Circuits

This tutorial provides ground theory and practical strategies for the design of clock-and-data-recovery circuits. We begin by relating performance metrics such as jitter transfer, jitter tolerance, and jitter peaking to CDR loop components and use these relationships to elucidate application-specific design challenges and tradeoffs. Following this, we will discuss both architectural- and circuit-level techniques to manage/overcome these tradeoffs. Specifically, we would compare different architectures: bang-bang vs. linear, digital vs. analog vs. hybrid loops, oscillator vs. phase interpolator, and reference-less vs. reference-based CDRs.

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Instructor: Pavan Kumar Hanumolu

Pavan Kumar Hanumolu is an Associate Professor in the Department of Electrical and Computer Engineering at the University of Illinois, Urbana-Champaign. He received the Ph.D. degree from the School of Electrical Engineering and Computer Science at Oregon State University, Corvallis, in 2006, where he subsequently served as a faculty member until 2013. Dr. Hanumolu's research interests are in energy-efficient integrated circuit implementation of analog and digital signal processing, wireline communication systems, and power conversion. He currently serves as an Associate Editor of the Journal of Solid-State Circuits, and is a technical program committee member of the VLSI Circuits Symposium, and International Solid-State Circuits Conference

T7: Basics of Many-Core Processors

This tutorial focuses on the design of many-core processors spanning clients to servers to high-performance computing systems in scaled CMOS process. Key circuits and design techniques are highlighted for robust and variation-tolerant logic, embedded memory arrays and on-die interconnect fabrics. Also presented are design principles that enable a wide dynamic voltage-frequency operating range, spanning multi-threaded high-throughput near-threshold voltage to single-threaded burst performance modes. Fine-grain multi-voltage design and power management techniques are covered, along with smart variation-aware workload mapping schemes to achieve maximum performance under stringent thermal and energy constraints. Real chip design examples are used to illustrate basic design principles and practical considerations.

Instructor: Vivek De

Vivek De is an Intel Fellow and Director of Circuit Technology Research in Intel Labs. He is responsible for providing strategic technical directions for long-term research in future circuit technologies and leading energy efficiency research across the hardware stack. He has 223 publications in refereed international conferences and journals and 195 patents, with 30 more patents filed (pending). He received an Intel Achievement Award for contributions to integrated voltage regulator technology. He received a Best Paper Award at the 1996 IEEE International ASIC Conference, and nominations for Best Paper Awards at the 2007 IEEE/ACM Design Automation Conference (DAC) and the 2008 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). One of his publications was recognized in the 2013 IEEE/ACM Design Automation Conference (DAC) as one of the "Top 10 Cited Papers in 50 Years of DAC". He received a Ph.D. in Electrical Engineering from Rensselaer Polytechnic Institute, Troy, New York. He is a Fellow of the IEEE.

T8: Analog Techniques for Nano-power Circuits

This tutorial presents the design methodology and examples of analog circuits having nanoampere consumption with application in systems with short activity periods followed long standby. They are essential for the area of energy harvesting where the amount of available energy can unpredictably change by orders of magnitude. Low load efficiency of power management becomes a very important parameter in a wide breadth of applications. Circuit examples include biasing, precision voltage references, oscillators, charge pumps, adaptive speed amplifiers and comparators, LDOs, DCDC converters.

Instructor: Vadim Ivanov

Vadim Ivanov received the MSEE and the Ph.D. in 1980 and 1987, respectively, both in the USSR. He designed electronic systems and ASICs for naval navigation equipment from 1980 to 1991 in St. Petersburg, Russia, and mixed-signal ASICs for sensors, GPS/GLONASS receivers and for motor control between 1991 and 1995. He joined Burr Brown (presently Texas Instruments, Tucson) in 1996 as a senior member of technical staff, where he has been involved in the design of the operational, instrumentation, power amplifiers, references, and switching and linear voltage regulators. He has over 80 US patents and applications on analog circuit techniques and authored over 30 technical papers and three books: "Power Integrated Amplifiers" (Leningrad, Rumb, 1987), "Analog system design using ASICs" (Leningrad, Rumb, 1988), both in Russian, and " Operational Amplifier Speed and Accuracy Improvement", Kluwer, 2004.

T9: Frequency Synthesizers for Wireless Transceivers

A frequency synthesizer is a key building block in wireless systems. The $\Delta\Sigma$ fractional-N PLL-based synthesizer plays a critical role in modern transceivers not only as a local oscillator but also as a phase modulator with direct digital modulation. However, the traditional PLL in advanced CMOS technology suffers from poor scalability, loop parameter variability, leakage current and linearity problems. Accordingly, diversified PLL architectures and circuit techniques have been recently proposed in consideration of performance, power and cost, thus making it more difficult than ever for circuit designers to choose the right design solution. This tutorial gives some insight into PLL basics tailored for circuit designers. Then, system perspectives and practical circuit design aspects for frequency synthesis will be presented.

Instructor: Woogeun Rhee

Woogeun Rhee is a Professor at Tsinghua University, China. He received the B.S. degree from Seoul National University in 1991, the M.S. degree from UCLA in 1993, and the Ph.D. degree from the University of Illinois, Urbana-Champaign, in 2001. From 1997 to 2001, he was with Conexant Systems, CA, where he was a Principal Engineer and developed low-power low-cost fractional-N synthesizers. From 2001 to 2006, he was with IBM Thomas J. Watson Research Center, NY and worked on clocking area for high-speed I/O serial links. In August 2006, he joined the faculty of Tsinghua University, China. He currently holds 19 U.S. patents.

T10: CMOS Sensors for 3D Imaging

3D imaging has become a hot research topic in the last few years, driven by the needs of emerging markets looking for next-generation user interfaces based on gesture control. Moreover, 3D vision systems offer amazing possibilities of improvement in many other areas like automotive, security and surveillance, cultural heritage preservation, ambient-assisted living, industrial control, etc., because they significantly increase the robustness of object classification with respect to conventional 2D imagers. This tutorial will introduce participants to the exciting field of 3D imaging, providing an overview about image-sensor architectures capable of distance measurement. An introduction to existing 3D imaging technologies will be given, addressing the peculiarities of each measuring technique and the possible application domains. The focus is on solid-state sensor architectures as enabling technologies to improve the performance of 3D vision systems, with a particular emphasis on time-of-flight implementations. Finally, participants will get some practical tools such as figures of merit and experimental characterizations guidelines for a comprehensive comparison of 3D imager performance and a perspective toward the future challenges in this fast-evolving field.

Instructor: David Stoppa

David Stoppa received the Ph.D. degree in Microelectronics from the University of Trento, Italy. He is the head of the Integrated Radiation and Image Sensors research unit at FBK where he has been working as a research scientist since 2002 and as group leader of the Smart Optical Sensors and Interfaces group from 2010 to 2013. His research interests are in the field of CMOS image sensors and biosensors. He has published more than 100 papers, and holds several patents in the field of image sensors. He is currently a member of the ISSCC ITPC and was technical committee member of 'International Image Sensors Workshop' in 2009 and 2013. Dr. Stoppa received the 2006 ESSCIRC Best Paper Award.

F1: *High-Speed Interleaved ADCs*


Organizer: **Stéphane Le Tual,** *STmicroelectronics, Crolles, France*

Co-organizer: **Borivoje Nikolic,** *University of California, Berkeley, CA*

Committee: **Tetsuya Iizuka,** *University of Tokyo, Tokyo, Japan*
Ichiro Fujimori, *Broadcom, Irvine, CA*

Time-interleaved ADCs have become critical components in high-speed wireline and wireless communication systems. This forum will deliver a comprehensive treatment of state-of-the art design techniques for high-speed interleaved ADCs. Topics include transistor-level design techniques, calibration (estimation & correction), as well as the link between system specifications and required ADC performance.

Interleaved ADCs Through the Ages
Ken Poulton, *Keysight Laboratories, Santa Clara, CA*
Research on interleaved samplers and ADCs goes back to work first published in 1980 by Hewlett Packard and UC Berkeley. Products such as oscilloscopes used small numbers of interleaved ADCs to reach the highest sampling rates available in the 1980s and 1990s. In 2002, the massive time-interleaving revolution was kicked off, which later gained further momentum with low-power ADC slice architectures such as SARs. Frequency interleaving provides another recent technology branch. This talk will present the history of ADC interleaving, focusing on major achievements and some of their problems and the solutions that were invented to solve them.

Ken Poulton received a B.S. in Physics and an M.S. in Electrical Engineering from Stanford University in 1980. He then joined Hewlett-Packard Laboratories (now Keysight Laboratories in Santa Clara, CA) where he has developed integrated circuits for data conversion in GaAs MESFET, GaAs HBT, silicon bipolar, BiCMOS and CMOS technologies. He became a project manager in 2000; he is now a master engineer. Ken has published papers on eight "world's-fastest" data converters, including "A 1 GHz 6-bit ADC System," which won the JSSC Best Paper Award for 1987. He was a member of the ISSCC International Technical Program Committee and a Guest Editor for JSSC. He holds 11 patents and is an IEEE Fellow.

Mismatch Error Correction for High-Resolution, GS/s Time-Interleaved ADCs
Per Löwenborg, *Signal Processing Devices, Linköping, Sweden*
After more than 35 years of research and development, the level of commercial and academic interest in time-interleaved ADC arrays is now higher than ever. With the possibility to extend the sampling rate beyond the limits of single-core ADCs, time-interleaving is now being deployed in high-resolution ADC designs. However, mismatch between the ADCs in the array and the resulting aliasing distortion that degrades the effective resolution is a challenge in these systems.

This presentation compares a select set of methods for mismatch error correction and highlights some possibilities and limitations. These methods involve the process of reconstructing new samples with less aliasing distortion as well as techniques for computing estimates of the mismatch needed for the correction. Measurement results of digital mismatch error correction applied to high-resolution time-interleaved GS/s ADC arrays are presented. Finally, the close connection between I/Q-balancing in quadrature demodulators and mismatch error correction in time-interleaved ADC is illustrated.

Per Löwenborg was born in Oskarshamn, Sweden, in 1974. He received Ph.D. and Docent degree in Electronics Systems from Linköping University, Sweden, in 2002 and 2009, respectively. He has more than 15 years post-graduate experience in R&D work within the field of analog and digital filters and filter banks, data converters, and signal processing enhancement of mixed-signal circuits. He is the author or co-author of about 75 international journal and conference papers, one textbook, and holds four patents. He was awarded the 1999 IEEE Midwest Symposium on Circuits and Systems best student paper award and the 2002 IEEE Nordic Signal Processing Symposium best paper award and has served as Associate Editor for IEEE Signal Processing Letters. Since 2006, Dr. Löwenborg is Chief Technology Officer at Signal Processing Devices Sweden AB which is an electronics company specializing in signal-processing enhancement solutions of analog and mixed-signal circuits as well as high-performance digitizers.

Highly Accurate Adaptive Digital Calibration for High-Speed High-Resolution Time-Interleaved ADC
Takashi Oshima, *Hitachi, Tokyo, Japan*
Purely digital post-calibration for time-interleaved A/D converters is presented with theoretical analysis and experimental results. It can correct all kinds of mismatches (gain, DC offset, sampling timing and bandwidth) among sub-converters assisted by the reference converter. It can compensate for the higher-order effects of sampling-timing and bandwidth mismatches with minimum complexity, which is essential to achieve both very-fast sampling rates and very-high effective resolution. The proposed calibration technique works successfully for both Nyquist-sampling and sub-sampling time-interleaved A/D converters. Therefore, it can be applied to both direct-sampling and direct-sub-sampling next-generation receivers.

Takashi Oshima received B.S., M.S. and Ph.D. in physics from University of Tokyo in 1996, 1998 and 2001, respectively. He joined Central Research Laboratory of Hitachi Ltd. in Tokyo in 2001, where he has been developing A/D converters, PLL, wireless-transceiver circuits and various sensor circuits. He developed many commercial ICs so far including the RF-ICs for Bluetooth, UHF RF-ID readers and multi-mode cellular phones. From 2005 to 2006, he was a visiting researcher at Berkeley Wireless Research Center of University of California at Berkeley, USA, where he made a research on digitally assisted A/D converters. From 2009 to 2012 he served as treasurer and secretary of IEEE Solid-State Circuits Society Japan Chapter. As the secretary of IEEE Solid-State Circuits Society Japan chapter, he organized several technical meetings and seminars in Japan. He currently serves as a Technical Program Committee member of ESSCIRC. He is a co-recipient of 2010 Best Invited Paper Award of IEICE Electronics Society in Japan and a co-recipient of 2003 R&D 100 Award from R&D Magazine. He also received the contribution awards from IEICE in 2011 and 2013. He holds 7 patents of wireless transceivers and PLL and 8 patents of A/D converters. His current research interests include the next-generation wireless transceiver design and the digitally assisted A/D converters. He is a member of IEEE, IEICE and Physical Society of Japan.

ADC Interleaving Errors Corrected by Adaptive Post-Processing
Asad Abidi, *University of California, Los Angeles, CA*
All interleaving errors express themselves with a particular structure in the frequency domain. By extending well-known methods of adaptive interference cancellation, errors can be detected and suppressed using only digital signal processing at the ADC output. The system adapts rapidly on sets of discrete tones, but requires sophisticated sub-band adaptation and coefficient diffusion to track wideband stationary waveforms.

Asad Abidi is Distinguished Professor of Electrical Engineering at UCLA. He is Fellow of IEEE and Member of the National Academy of Engineering.

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Specifications vs. Applications: Driving Architectural Choices

Aaron Buchwald, *InPhi, Irvine, CA*

Time interleaving gives designers an additional degree-of-freedom to solve problems of achieving ultra-fast quantization at reasonably high resolution. The technique is not free and certainly not without problems. For as soon as multiple paths are encountered in the signal chain, a myriad of errors become apparent, often glaring. It turns out that in a non-interleaved ADC, a lot of non-idealities hid under our noses, but were "mixed" to DC where we weren't even aware they existed. Multi-path design modulates these "hidden" errors and their harmonics with sub-multiples of the sample rate quickly producing a "spur farm."

Mitigating all possible time-interleaved errors comes at a heavy cost in complexity, risk, power and performance. Knowing which errors are most important and which can be neglected in any given application is essential for picking an appropriate architecture and calibration scheme. This talk will review specification requirements for various applications where time-interleaved ADCs might be used. Different types of error sources will be treated separately to determine their impact on overall system performance. Careful analysis of all classes of errors will ultimately drive key decisions and trade-offs in the choice of architecture, digital signal processing and circuit design.

Aaron Buchwald has 32 years experience in the field of analog integrated circuit design. He is currently a Fellow at Entropic Communications after the acquisition of Mobius Semiconductor, where he was CEO and founder. Prior to Mobius, Dr. Buchwald worked at Broadcom, where he helped build a world-class analog team emphasizing design in a mixed-signal environment. Dr. Buchwald's work on embedded CMOS Analog-to-Digital Converters (ADCs) enabled the production of single-chip cable set-top boxes and cable modems with integrated analog front ends and DSP circuitry. His work with Klaas Bult was awarded the best paper prize in 1997 at ISSCC. Later, Dr. Buchwald was responsible for development of high-speed serial transceivers (XAUI, CX4 and Fiber Channel) at Broadcom. The initial XAUI transceivers were some of the first to employ adaptive receive equalization. Dr. Buchwald was formerly an Assistant Professor at the Hong Kong University of Science and Technology (HKUST). In his early career, Dr. Buchwald spent two years as an analog IC designer at Siemens in Munich, Germany. Prior to that, he spent four years at Hughes Aircraft Company in El Segundo, CA. Dr. Aaron Buchwald was born in Ames, Iowa and received a B.S.E.E. from the University of Iowa, Iowa City, Iowa, and an M.S. and Ph.D. from the University of California, Los Angeles. He is co-author of the book Integrated Fiber-Optic Receivers. He has taught professional short-courses and tutorials on data converters and serial transceivers.

GS/s Time-Interleaved ADCs for Broadband Multi-Carrier Signal Reception

Kostas Doris, *NXP, Eindhoven, The Netherlands*

Today's low-to-medium resolution extensively interleaved analog-to-digital converters (ADC) are an excellent fit for the conversion of GHz broadband signals. They are amalgams of algorithmic concepts and circuit techniques that adapt the successive-approximation search algorithm to the properties of nanometer CMOS technologies. But, are extensively interleaved ADCs capable to meet the challenges posed by multi-carrier communication and radar applications that typically require very low noise and spurs, absence of signal images, high linearity, and large bandwidth?

This presentation starts by showing the impact of time interleaving on the conversion of multi-carrier broadband signals, such as those encountered in cable and short-range wireless communication systems. Key circuit issues and design tradeoffs are then presented, linking them to the properties of multi-carrier signal reception using the DOCSIS standard as an example. The presentation then shows how the introduction of architectural concepts such as hierarchy, redundancy, frequency translation and extensive digital calibrations can offer new degrees of freedom to enable low power GS/s broadband multi-carrier signal reception.

Kostas Doris was born in Thessaloniki, Greece in 1973. He received the M.Sc. Physics and Radio-Electronics degrees from Aristotle University of Thessaloniki, Greece, in 1996 and 1998, respectively. In 2004, he received his Ph.D. degree from the Technical University of Eindhoven, The Netherlands. He joined Philips Research in 2003, and subsequently NXP Semiconductors in 2006. He is currently heading the department of High-speed Data Acquisition in Central Research & Development in NXP. His area of interest includes high-speed high-resolution data converters, mm-wave receivers and high-speed serial interfaces. He is the author and co-author of a multitude of papers, patents and books in the field of data converters.

Embedded CMOS ADCs for Optical Communications

Yuriy M. Greshishchev, *Ciena, Ottawa, Canada*

Optical communications has been undergoing revolutionary transformations, where CMOS DSP ASICs and embedded interleaved ADCs are main reason for its success. Time interleaving is a holy grail of CMOS design to satisfy high sampling rate requirements. Less known and popular is frequency interleaving, which tackles the bandwidth limitations. Potentially, these two interleaving techniques may help to fulfil ever-rising requirements for the optical communication ADCs.

Yuriy Greshishchev received the M.S.E.E. in 1974 and Ph.D. in 1985, both in the Ukraine. He held a Post- Doctoral Fellow position at the University of Toronto, Canada in 1994-1995. He joined Nortel (now Ciena), Ottawa, Canada in 1996, where he is currently a Sr. Technical Advisor and Data Converter Architect for optical transport product. His frontier contributions to multi-gigabit SiGe and CMOS circuits reflected in numerous IEEE SSCS publications, workshops, and tutorials. Dr. Greshishchev served on the ISSCC International Technical Program Committee (2001-2009). He was a Guest Editor for the IEEE Journal of Solid-State Circuits (Dec. 2005). Dr. Greshishchev was co-recipient of an ISSCC 2008 award for the panel topic "Trends and Challenges in Optical Communications Front-End." He is now a TPC member for the Compound Semiconductors IC Symposium.

F2: *Memory Trends: From Big Data to Wearable Devices*

Organizer: **Jonathan Chang,** *TSMC, Hsinchu, Taiwan*

Committee: **Jonathan Chang,** *TSMC, Hsinchu, Taiwan*
Leland Chang, *IBM, Yorktown Heights, NY*
Antoine Dupret, *CEA Leti-LIST, Gif-sur-Yvette, France*
Chulwoo Kim, *Korea University, Seoul, South Korea*
Fatih Hamzaoglu, *Intel, Hillsboro, OR*
Takefumi Yoshikawa, *Panasonic, Kyoto, Japan*

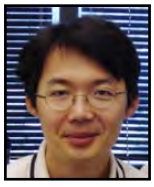
Memory continues to be a critical element in the full range of VLSI applications from big data to mobile applications to wearable devices. Recent trends, including process technology scaling limits, new memory applications, and evolving high-performance and low-power requirements, have driven the development of emerging memories. As both discrete and embedded memory scaling becomes ever more challenging, there is a widespread effort to look for alternative memory technologies to replace the entrenched SRAM, DRAM, or Flash. This forum brings together systems designers to discuss memory needs for future applications and memory designers to describe the latest developments in emerging and next generation memories. The first three speakers summarize memory requirements from a system perspective to cover a broad range of applications, including servers, data-centric computing, clients, notebooks, tablets, watches, glasses, and thermostats. The fourth speaker describes general design challenges for emerging memory in embedded systems to bridge to the second half of the program, which considers specific memory technologies. Two speakers will then present the challenges and solutions for Flash and DRAM scaling while the last two speakers will highlight the latest developments in MRAM and RRAM.

Memory Requirement Trends and Challenges: Servers to Devices
Suresh Chittor, *Intel, Hillsboro, OR*
Memory hierarchy is an essential part of any computing platform and the right memory architecture makes the system efficient and competitive. Memory architecture based on DRAM technology continues to evolve to meet increasing requirements on performance, cost, power and form-factor. Memory requirements across different platforms help drive innovations in technology and architecture. In this presentation, we start by reviewing key requirements and their trends across different platforms. We show several challenges we face in the near future. We look at future requirements in a different manner than usual by combining multiple traditional requirements. For example, bandwidth and capacity requirements need to be considered together instead in isolation. Bandwidth to capacity ratio can be an effective parameter for both requirements and solutions. Power efficiency in pJ/b will become more important and depends on bandwidth and power requirements. Form factor requirements have to look at CPU and memory together, instead of just the memory modules. These new requirements can be a better guide to evaluate alternate memory architectures likely to emerge in near future.

Suresh Chittor has been with Intel Corporation for more than 23 years. During his career, he has successfully lead many mainstream Intel products from concept to production. He has been a silicon architect, platform architect and engineering manager. He lead engineering of MCH for the first widely successful 4S Xeon servers launched in 1998 and server chipset architectures until 2005. Since 2005, Suresh has co-directed workstation and server platform definitions to meet customer requirements and bring in appropriate new technologies. He was staff architect for the latest Xeon servers. For the last 3+ years, he has been directing memory architecture for future Intel products spanning phones, tablets and servers. Suresh has been issued several patents in memory architecture, bus protocols and error handling. Suresh has a Ph.D in computer science from Michigan State University and an M.S. in computer science and engineering from Indian Institute of Science.

Memory System Requirements for the Big-Data Application Data-Centric Computing
Ken Takeuchi, *Chuo University, Tokyo, Japan*
This presentation overviews the memory system requirements for the big-data applications. In the conventional processing-centric computing such as PCs and HPC servers, the data amount was restricted and the key technological issue was to enhance the processing capabilities by increasing the clock frequency of CPUs and increasing the parallelism with multi/many cores. On the other hand, in the big data applications such as OLTP and OLAP, 3V (volume, variety and velocity) data must be handled. Thus, the key challenge is to reduce the cost of moving data through the deep memory hierarchy from the storage through the main memory to the CPU and eventually to resolve the Von Neumann bottleneck. This presentation discusses the memory system requirements especially emphasizing the storage class memory in such a data-centric computing architecture. The memory requirements for local IoT/wearable devices are also discussed. Finally, the impacts of the future fog/edge computing on the memory system are discussed, where the data are overflowed and a majority of the data are stored/processed at the edge of the network.

Ken Takeuchi is a Professor at the Department of Electrical, Electronic, and Communication Engineering of Chuo University. He is now working on database storage systems for big-data application, VLSI circuit design, signal processing and devices such as the emerging non-volatile memories, 3D-integrated SSDs, low-power 3D-LSI circuits and ultra low-voltage SRAMs. Before joining Chuo University, he was an Associate Professor at the University of Tokyo from 2007 to 2012. From 1993 to 2007, he lead Toshiba's NAND Flash memory circuit design team and commercialized six of the world's highest-density Flash memory products. He holds 220 patents worldwide. He won the Takuo Sugano Award for Outstanding Paper at ISSCC 2007. He has served on the program committee member of International Solid-State Circuits Conference (ISSCC), Symposium on VLSI Circuits, Asian Solid-State Circuits Conference (A-SSCC), International Memory Workshop (IMW) and Non-Volatile Memory Technology Symposium (NVMTS).



Memory and Storage Requirement and Trend for ChromeOS
Eric Shiu, *Google, Mountain View, CA*
Internet and mobile application have been driving the semiconductor industry forward in the past 10 years. It's also known that memory and energy walls have been limiting the continuous scaling of compute horsepower. The other important consideration that keeps many of us awake at night is the user's privacy and data security. Of course, there is the war, disease and climate change that will put humanity in jeopardy, but that's beyond the scope of today's forum. We focus on the memory and storage requirement for today and future consumer devices, such as notebooks, tablets, watches, glasses or thermostats. We start with the user's desire for speed, simplicity and security at the application level, such as video capture, YouTube streaming, Hangout video call, online banking or fitness. Then break down to what it means to programmers, system architects, technologists and engineers. Finally, we discuss a few future research areas in memory architecture, technology and circuit design.

Eric Shiu is currently a chip lead at Google's consumer hardware group, specializing in SoC memory architecture. He received the M.S.E.E. degree from Stanford University in 1998. He was a custom circuit and RTL designer at Sun Micro's UltraSPARC group from 1998 to 2004. He was a principal engineer at PA Semi's SoC group responsible for I/O memory, L2 cache architecture and foundry technology from 2004 to 2008. He was a design lead in Apple's A-series SO\oC team from 2008 to 2014. He has authored and co-authored 20+ patents in the area of memory circuits and architecture.

Emerging Memories in Embedded Systems: Opportunities for the Digital Architect, Challenges for the Designers
Fabien Clermidy, *CEA-Leti, Grenoble, France*
The data deluge due to the explosion of embedded systems has drive requirements for larger memories. While logic functions have greatly evolved from year to year, improving much further than technology evolution, memories seems to stay quite stable, gently following Moore's law. As a result, memories are nowadays considered as the bottleneck of many systems and techniques: they limit power management strategies and represent a large part of power consumption; they limit performance due to their long access time and/or insufficient bandwidth and/or insufficient capacity; they imply a large area overhead due to memory duplication through cache mechanisms. In this context, we discuss how emerging memories can change the current status. More precisely, the following topics will be addressed:

- How CBRAM can help reduce power and open up new applications for FPGA.
- Challenges in integrating CBRAM and OXRAM technologies in Internet-of-Things circuits: architecture versus design trade-offs.

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- Memory crossbars: how RRAM can help solve big data problems by simplifying the memory hierarchy and what are the design challenges.
- Some perspective: what about integrating logic in memories? The logic-in-memory concept, benefits and issues.

Fabien Clermidy obtained his master degree in 1994, his Ph.D. in Engineering Science from INPG, Grenoble in 1999 and his supervisor degree from INPG in 2011. Fabien is a pioneer in designing Network-on-Chip based multi-core and was the integrator of the first asynchronous-based Network-on-Chip published at ISSCC in 2007. He then took the lead of the second generation of Network-on-Chip based multicore dedicated to 3GPP-LTE applications published at ISSCC in 2010 and was the leader of the CEA team which has been working on the P2012 multi-core architecture in collaboration with STMicroelectronics and ST-Ericsson. At this period, his team elaborated one of the first 3D multi-core prototypes embedding a WIDE-IO DRAM memory called WIOMING. Fabien is currently director of the digital design laboratory at CEA-LETI working on multi-core architectures and design with a focus on emerging technologies. In this position, he managed the team demonstrating the best performing low-voltage DSP developed in FDSOI technology and demonstrated at ISSCC in 2014. The team is also implied in the development of new architectures using emerging technologies such as 3D TSV, 3D monolithic integration and emerging memories such as RRAM. Fabien has published 2 books, more than 70 journal and conferences papers and is author or co-author of 15 patents. He is currently Associate Editor of TCAS-I journal.

3D NAND Flash: from Enterprise to Embedded Storages
Ki-Tae Park, *Samsung, Hwasung, South Korea*
Samsung created the world's first 3D V-NAND Flash memory in mass-production in 2013 and the first-generation product using 24-layers was developed mainly for enterprise storage application due to its high performance and endurace, which was reported at ISSCC 2014. One year after the announcement of 3D V-NAND, a newly developed 2nd generation of 3D V-NAND with 32-layers is now in mass-production in 2014 and its application is expanded into consumer SSD and embedded storage applications. This presentation overviews the mass-produced 3D V-NAND and some major challeneges that we have overcome. It also presents some important features that help take advantage many of the 3D V-NAND advantages.

Ki-Tae Park received the B.S. degree in electronics engineering from Kyoungbook National University, Korea, in 1993, and the M.S. and Ph.D. degree in machine intelligence and system engineering from Tohoku University, Japan in 1993, and 1999, respectively. From 1999 to 2001, he served as Research Associate and worked on Nano-CMOS devices, low power circuits, 3-dimensinal shared memories and artificial retina chips in Tohoku University. From 2001 to 2004 he joined Halo LSI in New York in circuit design for high-speed embedded flash and NAND compatible high density Flash memories using SONOS technology. He joined Samsung Electronics, Korea in 2004 and has working on design of MLC and TLC NAND flash memory products. He was responsible for designing world's first TLC NAND for SSD application. He was also respnsible for developing world's first 3D NAND product using vertical layer-stacking technology. He is currently a vice president and received several achievement awards from Samsung for his outstanding work and holds over 100 US patents.

Addressing Future Memory Challenges with Device Abstraction
J. Thomas Pawlowski, *Micron, Boise, ID*
Numerous papers and talks have discussed the many challenges of continuing the cost scaling of DRAM and other memory types. Each successively smaller node feature size compounds the issues. There will be an inevitable transition from currently used memory technologies to some replacement technology such as DRAM possibly being replaced by STT-RAM. Such a transition will occur sooner than the entire memory ecosystem is able to respond and with unpredictable suddenness. This talk identifies some of the challenges faced in the normal course of scaling. It examines some potential characteristics of future technologies and highlights the incompatibilities. It proposes how a seamless transition can be undertaken to allow all memory suppliers and consumers gracefully transition between technologies and simultaneously improve the products on both sides of the equation.

J. Thomas Pawlowski is a Fellow and Chief Technologist with Micron's Architecture Development Group. His responsibilities include evaluating new technologies and investments, exploring new memory and system architectures, and providing guidance to many technical teams, both internally and external to Micron. Mr. Pawlowski's experience includes the creation or co-creation of numerous groundbreaking memory architectures and concepts including: synchronous burst pipelined SRAM; hierarchical cache systems; Zero Bus Turnaround SRAM; abstracted memory; the first double data-rate memory (starting with SRAM and extending to DRAM and NAND technologies); Pseudo-Static RAM; high-speed NAND; the first double address rate memory; the first quad data rate memory; the first multi-channel memory; memories on SerDes buses; RLDRAM (the first DRAM to exceed SRAM performance); refresh and error-correction schemes for memory subsystems; the first 3D memory concept; root hardware architecture of Micron's newly announced nondeterministic Finite Automata Processor; and other projects still in development. Mr. Pawlowski earned a B.A.Sc. in electrical engineering, *summa cum laude,* from the University of Waterloo in Canada. He has well over 100 U.S. and in-flight patents and serves on several advisory boards and conference program committees. In his spare time, Mr. Pawlowski designs and builds loudspeakers, custom tools, and he has completed 60% of the design of a revolutionary electric car concept.

Technology Trends and Applications of MRAM from Big Data to Wearable Devices
Shinobu Fujita, *Toshiba, Kawasaki, Kanagawa, Japan*
Advancement of MRAM technologies will be shortly overviewed to clarify their advantages such as a high-speed access, a novel scalability and "normally-off and instant-on mode". Next, various applications from big data to wearable devices will be presented, and issues regarding their applications will also be explained.

Shinobu Fujita received Ph.D. degree from University of Tokyo in 1989. He joined Toshiba in 1989. He has been working for new applications based on nonvolatile memories for over 10 years. Currently, he is a Chief Research Scientist of Toshiba Corporate R&D Center and leading a project for development of STT-MRAM for ultra-low power and high-performance processors or SoC.

RRAM for Data Abundant System Technology: Managing Expectations and Minimizing Disappointments
Malgorzata Jurczak, *IMEC, Leuven, Belgium*
Resistive RAM has attracted significant attention in recent years due to growing demand for faster, highly scalable, low power and cost-effective non-volatile memory solutions for mass storage applications. This has resulted in significant research activities to explore numerous resistive switching mechanisms among which oxygen vacancy conductive filament in OXRAM and metallic conductive bridge in CBRAM seems to be the most promising. In this presentation, the latest developments of RRAM technology (OXRAM and CBRAM) and its current state-of-the-art will be discussed in details. The promising attributes and key scientific and technological issues in bringing this technology to the manufacturable level will be identified. The presentation will cover single bit design for low current operation, scalability, process integration and some aspects of 1S1R cell design.

Malgorzata Jurczak has been the Director of Emerging Memories Program at IMEC, Belgium since 2011. She received M.Sc. and Ph.D. in electrical engineering from the Warsaw University of Technology, Poland. She started her research career in the field of modelling of advanced CMOS devices in the Institute of Microelectronics and Optoelectronics of Warsaw University of Technology, Warsaw. In 1998 she joined CNET, France Telecom where she participated in research on CMOS device architectures for 0.18 and 0.12µm including strain-Si channels, SiGe and Ge gate, vertical transistor, localized SOI devices (silicon-on-nothing). In 2000 she joined IMEC where she was leading the IMEC-Philips Joint Development Program on 90nm and 65nm CMOS. In 2003 she became the manager of EMERALD program addressing design and fabrication of FINFET devices. In 2008 she became a manager of Memory Program (including Flash, DRAM MIM Capacitor, FBRAM and RRAM). She holds 20 patents, and has authored and co-authored more than 600 publications and conference contributions. She has been a member of technical committees of IEDM, IEEE SOI, ESSDERC, VLSI TSA conferences, Symposium on VLSI Technology and ITRS Roadmap. Since 2011 she has been also the Editor of IEEE Electron Device Letters.

F3: *Cutting the Last Wire – Advances in Wireless Power*

Organizer: **Marco Berkhout,** *NXP Semiconductors, Nijmegen, The Netherlands*

Committee: **Marco Berkhout,** *NXP Semiconductors, Nijmegen, The Netherlands*
Anton Bakker, *Integrated Device Technology, Morgan Hill, CA*
Christoph Sandner, *Infineon Technologies, Villach, Austria*
Wentai Liu, *UCLA, Los Angeles, CA*
Chih-Ming Hung, *Mediatek, Taipei, Taiwan*
Bill Redman-White, *University of Southampton, Southampton, United Kingdom*

In recent years the availability of products for wireless charging of mobile devices has increased rapidly. The introduction of the Qi standard for wireless power transfer has marked the beginning of what could be a revolution in the way we charge our smartphones and tablets. Wireless power transfer is considered for use in applications ranging from biomedical implants that require a couple of milliWatts to electrical vehicles that require kiloWatts. The vision of a future where we can conveniently, efficiently and safely charge our devices and vehicles anywhere without having to drag adapters and cables with us is gradually starting to become more realistic. This forum aims to give an overview of the state-of-the art in wireless power transfer. The fundamentals of different wireless power transfer techniques will be discussed, including not only inductive and resonant magnetic, but also capacitive power transfer and RF energy harvesting.

Wireless Power Transfer - Introduction and History
Grant Covic, *University of Auckland, Auckland, New Zealand*
The ability to provide power without wires was imagined over a century ago, but assumed commercially impractical and impossible to realise. However, for more than two decades the University of Auckland has been at the forefront of developing and commercialising this technology alongside its industrial partners. This research has proven that significant wireless power can be transferred over relatively large air-gaps efficiently and robustly. Early solutions were applied in industrial applications to power moving vehicles in clean room systems, roadway lighting, industrial plants, and in theme parks, but more recently this research has helped develop technology that has the ability to impact us directly at home. The presentation will describe some of the early motivations behind this research, and introduce some of the solutions that have been developed by the team of researchers at Auckland. It will also describe how the technology has recently been re-developed to enable battery charging of electric vehicles without the need to plug in, and alongside this how it has the potential to change the way we drive in the future.

Grant Covic received his BE (Hons), and Ph.D. degrees in Electrical and Electronic Engineering from The University of Auckland (UoA), New Zealand in 1986 and 1993, respectively. In 2013 he was appointed Professor within the Electrical and Computer Engineering Department at the UoA. In 2010 he co-founded (with Prof. John Boys) a start-up company "HaloIPT" focusing on electric vehicle (EV) wireless charging infrastructure. Presently he heads power electronics research at the UoA and co-leads the interoperability sub-team within the SAE J2954 wireless charging standard for EVs. His research interests include power electronics, electric vehicle battery charging and inductive power transfer (IPT) from which he has published more than 100 refereed papers in international journals and conferences. He holds a number of US patents with many more pending, from which licenses in specialized application areas of IPT have been granted around the world. He is a Fellow of the Institution of Professional Engineers New Zealand, a senior member of IEEE, and has been awarded the New Zealand Prime Minsters Science Prize, the KiwiNet Research Commercialisation Award and the Vice Chancellors Commercialisation Medal for his work in IPT.

Capacitive Power Transfer – Efficient Power and Data
Seth Sanders, *University of California, Berkeley, CA*
With the formation of the Qi standard, wireless charging is gaining momentum in changing the way we provide power to devices. The Qi standard is based on an inductive interface, shared between the power transmitter, and a portable device. However, another approach exists in the form of a capacitive interface, formed by two metal plates separated by a thin layer of isolation. In comparison to an inductive interface, a capacitive interface is more limited in separation distance but also has much reduced external fields, a single resonance, and no need for substantial reactive magnetizing current. The main attractiveness of wireless charging is the absence of cables and wires. However, one important aspect still absent is the data communication. Most existing capacitive power and data technology is either very near field with sub-mm range for chip-to-chip applications, or for biomedical applications where the data rate is low. The presentation will review the basic physics, constraints, and representative circuit approaches to capacitive power transfer. Examples from on-going work will be discussed, that aim to fully extend the USB interface to the contactless domain.

Seth R. Sanders is a Professor of Electrical Engineering in the Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. He received S.B. degrees (1981) in Electrical Engineering and Physics, and the S.M. (1985) and Ph.D. (1989) degrees in Electrical Engineering from the Massachusetts Institute of Technology, Cambridge. His research interests are in high-frequency power conversion circuits and components, design and control of electric machine systems, and nonlinear circuit and system theory. Dr. Sanders is co-founder, and presently serving as CTO of utility flywheel energy storage company Amber Kinetics Inc., Union City, CA. Dr. Sanders received the NSF Young Investigator Award in 1993 and multiple Best Paper Awards from the IEEE Power Electronics and the IEEE Industry Applications Societies. He is presently Chair of the IEEE PELS Technical Committee on Power Systems and Components. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-At-Large of the IEEE PELS Adcom. He is an IEEE Fellow and a Distinguished Lecturer of the IEEE PELS.

Midfield Powering for Bioelectronics Medicines
Ada Poon, *Stanford University, Stanford, CA*
Sensors are capable of precisely monitoring and recording activity in the human body, providing feedback to directly modulate neural activity and physiological functions; thus hold promise for treating a broad range of diseases. To implant these devices in the body, they need to be miniaturized. New energy harvesting methods are needed to miniaturize the last thing that makes these devices so large - the battery. In this talk, I will present a new method of electromagnetic energy transfer, termed midfield powering, to power devices at the scale of a millimeter or less anywhere in the body. In conjunction with innovations in low-power integrated circuit design, the processing capabilities of a network of these devices are virtually unlimited. I will therefore conclude the talk on how our approach allows for new electroceutical devices where diseases are treated with electronics rather than drugs.

Ada Poon received her B.Eng. degree from the EEE department at the University of Hong Kong, and her M.S. and Ph.D. degrees from the EECS department at the University of California at Berkeley. Her dissertation attempted to connect information theory with electromagnetic theory so as to better understand the fundamental limit of wireless channels. Upon graduation, she spent one year at Intel as a senior research scientist building reconfigurable baseband processors for flexible radios. Afterwards, she joined SiBeam Inc., architecting Gigabit wireless transceivers leveraging 60 GHz CMOS and MIMO antenna systems. After two years she joined the faculty of the ECE department at the University of Illinois, Urbana-Champaign. Since then, she has changed her research to integrated biomedical systems. In 2008, she moved back to California and joined the faculty of the Department of Electrical Engineering at Stanford University. She is a Terman Fellow at Stanford University. She received the Okawa Foundation Research Grant in 2010 and NSF CAREER Award in 2013.

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Wireless Power Delivery for Medical Applications

Chi-Ying Tsui, *The Hong Kong University of Science and Technology, Hong Kong, China*

Wireless power transfer (WPT) is widely considered for deployment in implantable medical devices (IMDs) to eliminate the use of battery. To reduce absorption by the human tissue, transmitter power should be reduced through improving the power transfer efficiency of the transmitter, the coupling coils and the receiver. In this talk, we will present our vision on the design of an energy-efficient wireless power transfer system for medical applications. On the receiver side, a reconfigurable rectifier is used so that through mode switching the output voltage could be upheld when the load and coupling conditions change without the need of increasing the transmitter power. On the transmitter side, a global control loop is used to adjust the transmitter power to adapt to load and coupling variations if the output voltage cannot be maintained through mode switching. Fast and energy efficient data feedback techniques through a wireless communication link will also be discussed.

Chi-ying Tsui received his B.S. degree in Electrical Engineering from the University of Hong Kong and Ph.D. degree in Computer Engineering from the University of Southern California in 1994. He joined the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology in 1994 and is currently a Full Professor in the department. His research interests includes designing VLSI architectures for low power multimedia and wireless applications, developing power management circuits and techniques for embedded portable devices, ultra-low power systems and energy harvesting applications. He has published more than 170 refereed publications and holds 10 US patents on power management, VLSI and multimedia systems. He received the best paper awards from the IEEE Transactions on VLSI Systems in 1995, IEEE ISCAS in 1999, IEEE/ACM ISLPED in 2007, and IEEE DELTA in 2008, CODES in 2012. He also received the Design Awards in the IEEE ASP-DAC University Design Contest in 2004 and 2006.

Comparison of Magnetic Charging Techniques for Mobile Devices

Matteo Agostinelli, *Infineon Technologies, Villach, Austria*

Wireless Power Transfer (WPT) is an increasingly popular technology in mobile applications, allowing the user to conveniently recharge the device without the need to carry battery chargers and wires. Moreover, the mechanical stress due to insertion of power plugs into the device is eliminated, therefore reducing the chances of a device failure. If the vision of a widespread distribution of wireless charging stations in public places will be fulfilled, users will be able to conveniently recharge their devices on-the-go. This presentation focuses on low-to-medium power applications, ranging from a few Watts up to 30W. Even though the underlying physical principles and the supporting circuitry remains fundamentally unaltered, different techniques can be applied and the designer of a WPT system is faced with multiple choices, e.g. resonant versus non-resonant operation, loose or tight coupling, and operating frequency range. In the presentation, these techniques will be compared, highlighting advantages and drawbacks, and it will be shown how the different competing standards, defined over the past years, are guiding the designer through these choices.

Matteo Agostinelli was born in Udine (Italy) in 1981. In 2006 he received the Laurea Magistrale (M.Sc.) degree in Electrical Engineering with honors at the University of Udine, Italy. From 2006 to 2008 he worked as a research assistant at the University of Udine, focusing on low-power techniques for digital CMOS circuits and nanoscale innovative devices (Multi-Gate FETs, FinFETs). In September 2008 he started his Ph.D. work in the Institute of Networked and Embedded Systems at the University of Klagenfurt (Austria) in cooperation with Infineon Technologies and Lakeside Labs, focusing on nonlinear control techniques for DC-DC converters. He was the recipient of the Best Student Paper award at IEEE MWSCAS 2010. In September 2012 he joined Infineon Technologies, where he is currently working on the development of battery and power management mixed-signal SoCs.

Magnetic "Inductive" Charging and the Qi standard

Dries van Wageningen, *Philips Research, Eindhoven, The Netherlands*

The Wireless Power Consortium (WPC) started in December 2008, released the first Qi specification (v1.0) in August 2010 the second one (v1.1) in May 2012. The Qi standard is based on the principle of a loose magnetic coupling between a primary coil and a secondary coil. In the first release the size and distance between primary and secondary coil have been limited to ensure a low stray field and therefore a low EMF exposure to the environment. Nowadays the media has labeled the Qi technology as "inductive coupling" with limited spatial freedom in contrary to "magnetic resonance" with more spatial freedom. However the Qi technology has been specified to be resonant from the early start. The evolution of the Qi standard towards larger spatial freedom (v1.2) is therefore just a matter of using the already available resonance properties. The presentation will give an overview of the initial Qi specification and the evolution steps (v1.1) towards a standard (v1.2) that covers a broad spectrum of possibilities while keeping backwards compatibility with the installed base.

Dries van Wageningen is senior scientist at research Philips and has been active for the Wireless Power Consortium (Qi) since the start in December 2008. He has made several proposals for the Qi specification, including major contributions on the Communication & Control protocol and on Foreign Object Detection. In previous work he was heavily involved in scalable and distributed communication systems. The knowledge accomplished in this work, gives him an excellent base to address the interaction protocol of a wireless power system and enables him to tackle the essential aspects of an evolving industrial standard.

Magnetic Resonant Charging and the A4WP Standard

Francesco Carobolante, *Qualcomm Technologies, San Diego, CA*

As mobile devices demand more and more from the battery to support an "all-day" experience, recharging throughout the day has become a common occurrence. Wireless power technology offers the promise of seamless charging, a key to maintaining productivity, enabling such user-friendly use cases, which include charging multiple devices with differing power requirements (from wearable and mobile devices to tablets and notebooks) at the same time in the same charging area. This requires a wireless charging technology that can become a part of everyday activities and support flexible implementations. Wireless power transfer technology based on magnetic resonance can satisfy the flexibility and convenience that consumers have been looking for. The Rezence specification from the Alliance for Wireless Power (A4WP) maintains conformance to key system interface parameters and guarantees interoperability while maintaining the maximum freedom of design. This allows for an easier installation of wireless charging surfaces into everyday objects and form factors. In this session, we will analyze how the desired use cases affect wireless power technology requirements, specifications and standardization efforts, including regulatory constraints and consumer product definitions.

Francesco Carobolante is Vice President of Engineering at Qualcomm Incorporated. In this position, he has been responsible for the development of products and technologies for mixed signal Integrated Circuits (primarily in Power Management and analog subsystems). He is currently leading the development of Wireless Power Transfer technology and its standardization through A4WP (the Alliance for Wireless Power). Prior to joining Qualcomm, he held positions at STMicroelectronics, Tripath Technology and Fairchild Semiconductors, developing analog, power, and MEMS based mixed signal products. He holds more than 50 patents and has published several papers on power, mixed signal and system design. He received an Electrical Engineering and PE degrees from the University of Padova in Italy, and a MSEE from UCLA.

The Confluence of Resonant Switching Topologies and Wireless Charging

Sanjaya Maniktala, *Integrated Device Technology, Morgan Hill, CA*

We have been hearing a lot recently of magnetic induction (MI) wireless charging and resonant switching topologies, in particular the LLC topology. But are they really that different? In this presentation we will put them side-to-side as a means of appreciating and analyzing them even better, by comparing them. This strategy can give us great insight, besides helping reap the advantages and the accruing field experience of each, into the other, as well as avoiding pitfalls.

Sanjaya Maniktala is the author of five well-known books on power conversion, plus the only book on Power over Ethernet, published in 2013 by McGraw-Hill. He has over two decades of experience as an engineer, technical lead and manager, working in well-known companies in India, Singapore, Germany and USA. He currently works for Integrated Device Technology in San Jose as a product definer for their innovative wireless power charging chips, and holds several key patents including the floating buck regulator topology.

F4: *Building the Internet of Everything (IoE): Low-Power Techniques at the Circuit and System Levels*


Organizers: **Marian Verhelst,** *KU Leuven, Leuven, Belgium*
Dennis Sylvester, *University of Michigan, Ann Arbor, MI*

Committee: **Makoto Takamiya,** *University of Tokyo, Tokyo, Japan*
Mike Clinton, *TSMC, Austin, TX*
Kathy Wilcox, *AMD, Boxborough, MA*
Koichi Nose, *Renesas Electronics, Tokyo, Japan*

Current projections estimate there will be 25-30 billion devices on the Internet of Things (IoT) by 2020. While technology scaling no longer brings automatic system energy savings, emerging big-data and wearable-monitoring applications require compact autonomous devices. These divergent requirements steer research towards new energy efficiency strategies for compact wireless devices at the circuit (analog, digital), architectural, and system levels.

This forum brings together recent developments towards next-generation energy-scarce SoCs for wearables and the IoT, together forming the Internet of Everything (IoE). The speakers will cover recent low-energy strategies, including energy harvesting and power management techniques, novel processor and compute architectures, low-power memory options and smart integration approaches.

Low-Power Integrated Circuit and System Design for Wearable Healthcare Applications
Mario Konijnenburg, *imec / Holst Centre, Eindhoven, The Netherlands*

The impact of wearable technology and Internet of Things (IoT) is already felt everywhere. But perhaps the greatest potential lies in healthcare applications, as more and more people are interested in indicators that continuously show their health and fitness state. This opens up opportunities for the engineer to develop SMARTER and SMALLER wearable devices, such as smart watches and glasses, where low-power, multi-sensor support, reliable data, and low-cost are the key challenges.

This talk focuses on integrated circuit and system design for high-quality bio-medical data acquisition from a wide range of sensors. Topics that will be discussed are high sensitivity, low-power readout circuits, filters and accelerators to reduce noise and artefacts, data re-sampling, synchronization and feature extraction. Several system implementations, including commercially available ICs are reviewed and future directions are discussed.

Mario Konijnenburg received the M.S. degree in Electrical Engineering from Delft University of Technology in The Netherlands in 1993. He received the Ph.D. degree from Delft University of Technology in 1999 and his dissertation was entitled, "Automatic Test Pattern Generation for Synchronous Sequential Circuits". He joined Philips Research / NXP Semiconductors and worked on methodologies to improve testability of designs. Currently, he is system architect at Holst Centre / imec in Eindhoven, The Netherlands where he works on development of ultra-low power designs for biomedical applications.

Ambient Energy Harvesting for the Internet of Everything
Po-Hung Chen, *National Chiao-Tung University, Hsinchu, Taiwan*

The Internet of Everything (IoE) creates more relevant and valuable networked connections by linking people, data and things together through ubiquitous devices and facilities. Many of the IoE devices are extraordinarily small and need to be self-powered, harvesting energy from the environment to recharge the battery or to realize a battery-less system. Among various types of energy sources, thermal, solar, and RF energy are the most promising solutions for the IoE applications. The intermittent and limited power/voltage level of harvested energy, however, brings severe technical challenges in developing energy-efficient self-powered systems.

This talk discusses design considerations in ambient energy harvesting, system architecture and circuit design techniques, including maximum power-point tracking (MPPT), startup mechanisms, and low-power controllers. In addition, recent research trends in power management ICs for energy harvesting applications are presented.

Po-Hung Chen received the B.S. degree in Electrical Engineering from National Sun Yat-sen University, Taiwan in 2005, the M.S. degree in Electronics Engineering from National Chiao-Tung University, Taiwan in 2007, and the Ph.D. degree in Electrical Engineering from the University of Tokyo, Japan in 2012. In 2012, he joined Department of Electronic Engineering at National Chiao Tung University as an Assistant Professor.

Embedded Voltage Regulation and Energy Management for IoT/IoE
Gerard Villar Piqué, *NXP, Eindhoven, The Netherlands*

The Internet of Things presents difficult yet motivating challenges from the perspectives of system integration and low-power consumption, arising due to severe constraints in available space and energy. While the supply voltage of microelectronics systems has decreased to reduce power consumption, most of the energy storage components have not followed suit, in order to maintain their energy density. This talk will address embedded power converters (inductive or switched capacitor) that can bridge the gap between the energy sources and loads more efficiently than conventional LDOs, thereby contributing to the necessary power consumption reduction in systems meant to implement the Internet of Things. The most effective techniques (such as multi-ratio, modular converters) will be presented, as well as the main proposals from the state-of-the-art, commenting on their advantages and limits, and the different challenges that still need to be solved to make them fully suitable for application in the IoT/IoE. Important parameters, such as power efficiency and noise will be covered, as well as techniques to improve them.

Gerard Villar Piqué received the M.Sc. degree in 2001, and the Ph.D. degree in November 2007 from the Technical University of Catalonia, Barcelona, Spain. In April 2008, he joined the Mixed-Signal Circuits and Systems Group, at the Research Department of NXP Semiconductors, Eindhoven, The Netherlands. In his role as Principal Scientist of the High Voltage and Power Innovation Center, he is involved in research on integrated power-management systems. His main research areas include mixed-signal and analog microelectronics design, as well as power-management systems (including switched-mode power supplies), with special focus in low-power fully integrated switched-capacitor DC-DC converters. He has published a book on monolithic integration of inductive switching power converters, and he is a member of the Technical Program Committee of ESSCIRC.

Wearable Architectures: What IoT Means for Circuit Design
Rob Aitken, *ARM, San Jose, CA*

The world is entering a new era of vastly greater connectivity, where people interact with their environment in entirely new ways. Although "Internet of Things" is a broad term that can encompass almost any wireless technology, this talk will concentrate on wearable computing, looking at the range of technologies involved, the system issues to consider when designing such devices, power-management techniques, microarchitectural issues, and the circuits needed to support them. In addition, some of the challenges inherent in proliferating these devices will be considered, including establishing standards for security and interoperability.

Rob Aitken is an ARM Fellow and heads the Silicon portion of ARM R&D. His areas of responsibility include low-power design, library architecture for advanced process nodes, and design for manufacturability. His research interests include

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design for variability, defect analysis, and fault diagnosis. His group has participated in numerous chip tape-outs, including 6 at or below the 16nm node. He has published over 70 technical papers, on a wide range of topics. Dr. Aitken joined ARM as part of its acquisition of Artisan Components in 2004. Prior to Artisan, he worked at Agilent and HP. He has given tutorials and short courses on several subjects at conferences and universities worldwide. He holds a Ph.D. from McGill University in Canada. Dr. Aitken is an IEEE Fellow, and serves on a number of conference and workshop committees.

Memory Innovations for the Internet of Things
Sudhanshu Khanna, *Texas Instruments, Dallas, TX*
For the past decade, Internet of Things (IoT) applications have been driving research efforts across all areas of VLSI design from SRAM, non-volatile memory (NVM) to energy harvesting and sensor interfaces. However, only in the last few years have some IoT applications like metering and smart homes arisen as commercially viable targets for the semiconductor industry. This has resulted in development of new products specifically targeting ultra-low-power (ULP) and IoT applications. This talk begins by introducing commercial microcontrollers targeting IoT applications and the design decisions and techniques that help achieve their ULP goals. The rest of the talk focuses on SRAM and NVM design. We survey the state-of-the-art in SRAM and non-volatile memory design for IoT applications, looking at both bitcell and periphery design challenges. Autonomous IoT systems often need low-energy NVM accesses for data logging. We look at the unique features of ferroelectric RAM (FRAM) that help achieve these goals in current products and also comment on other NVM technologies that will drive success in the future.

Sudhanshu Khanna received his B.Tech. degree from Delhi College of Engineering, India in 2005 and his M.S. degree in Electrical Engineering from the University of Virginia in 2011. He joined Texas Instruments, Dallas in 2011 where he is currently a Senior Design Engineer in the Microcontroller Division. His research interests include SRAM design, ferroelectric-RAM design, and low-power system design methodologies. In his current role, he is working on the next generation of TI microcontrollers that can retain their state across a total power loss and wake up instantly without needing to boot-up. Sudhanshu was the winner of the IEEE ISSCC/DAC Student Design Contest 2011 and was elected Texas Instruments Innovator in Action for 2013. He has over 20 peer-reviewed publications and has filed over 40 US patents.

Nonvolatile Logic-in-Memory Architecture for Ultra-Low Power VLSI Systems
Takahiro Hanyu, *Tohoku University, Sendai, Japan*
In the Internet of Everything (IoE) era, ultra-low-power operation is necessary, as a result of the power limits of energy harvesting. Yet, it is also desirable to maintain high computational performance. An approach towards meeting these goals is to use "nonvolatile logic-in-memory" architectures, where nonvolatile storage elements are distributed over a logic-circuit plane. Magnetic tunnel junction (MTJ) devices exhibit good compatibility with present CMOS-based VLSI chips, and MJTs offer both low power and reduced interconnection delay because of a reduction in global interconnection count and volatile storage-element counts. As concrete design examples of nonvolatile logic-in-memory circuitry, I demonstrate a nonvolatile ternary content-addressable memory, an instant power-ON/OFF nonvolatile field-programmable gate array, and so on. I also describe a post-process variation-resilient logic-circuit design using MTJ devices.

Takahiro Hanyu received the B.E., M.E. and D.E. degrees in Electronic Engineering from Tohoku University, Sendai, Japan, in 1984, 1986 and 1989, respectively. He is currently a Professor in the Research Institute of Electrical Communication (RIEC), Tohoku University. His general research interests include nonvolatile logic circuits and their application to ultra-low-power and/or PVT-variation-free VLSI processors, and multiple-valued current-mode circuits and their application to power-aware asynchronous network-on-chip systems. He received the Sakai Memorial Award from the Information Processing Society of Japan in 2000, the Judge's Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002, the Special Feature Award at the University LSI Design Contest at ASP-DAC in 2007, the APEX Paper Award of the Japan Society of Applied Physics in 2009, the Excellent Paper Award of the IEICE, Japan, in 2010, the Ichikawa Academic Award in 2010, the Best Paper Award of the IEEE ISVLSI 2010, and the Paper Award of SSDM 2012. Dr. Hanyu is a Senior Member of the IEEE.

Smart Sensor Microsystems: Application-Dependent Integration Approaches
Minkyu Je, *DGIST, Daegu, Republic of Korea*
With the future filled with a trillion sensors on the way, there is a large variety in the forms of smart sensors for existing and future applications, such as environmental monitoring, smart grid, green transportation, smart home and building, wearables, implants, and so on. The applications of sensors and corresponding use scenarios define desired form factors, operation frequencies and durations, energy sourcing and management strategies, communication distances and data rates, as well as control interfaces and protocols, leading to significantly different microsystem structures and integration approaches. In this talk, I describe application-dependent microsystem structures and integration approaches, along with several examples of smart sensor microsystem integration across different applications. While on the one hand, we find the optimally crafted system designs and integration strategies can draw the maximum out of currently available technologies, the study on the other hand reveals the limitations, challenges, and bottlenecks of the technologies that must be overcome for a leap to the next stage of the sensor world.

Minkyu Je received the M.S. and Ph.D. degrees in Electrical Engineering from KAIST, Daejeon, Korea, in 1998 and 2003, respectively. In 2003, he joined Samsung Electronics, Giheung, Korea, as a Senior Engineer and worked on multi-mode multi-band RF transceiver SoCs for cellular standards. From 2006 to 2013, he was with IME, A*STAR, Singapore and led the Integrated Circuits and Systems Laboratory as a Department Head from 2011 to 2013. He was also a Director of the NeuroDevices Program from 2011 to 2013, and an Adjunct Assistant Professor at the Department of Electrical and Computer Engineering in the National University of Singapore from 2010 to 2013. Since 2014, he has been an Associate Professor at the Department of Information and Communication Engineering in DGIST, Daegu, Korea. His main research areas are advanced IC platform development, including smart sensor interface ICs and ultra-low-power wireless communication ICs, as well as microsystem integration leveraging the IC platform for emerging applications, such as intelligent miniature biomedical devices, ubiquitous wireless sensor nodes, and future mobile devices. He has more than 200 peer-reviewed international conference and journal publications. He also has more than 30 patents issued or filed.

Miniature IoT Sensor System Design and Integration Challenges
David Blaauw, *University of Michigan, Ann Arbor, MI*
This presentation focuses on the unique integration and system challenges of sensor devices composed of multiple heterogeneous die that achieve millimeter to centimeter form factors. Electrically, such miniature systems must operate with tiny batteries and harvesting capacity while physically, the integration of multiple die and passive components and system encapsulation poses significant challenges. We first describe the corresponding power management challenges, solutions, and trade-offs at the system level in such miniaturized devices. We then discuss a robust and energy efficient new interconnect standard, called Mbus, that is designed to connect multiple die in miniature sensor systems where pad space is limited. Practical concerns such as the initial charging, programming, and system booting of fully encased wireless systems will also be addressed, including programming and synchronization techniques using ultra-low-power wakeup receivers. We will also discuss encapsulation techniques to hermetically seal the system and isolate it from ambient factors, including light, which strongly impacts ultra-low power circuits. Several complete millimeter systems will be used to highlight the discussed techniques.

David Blaauw received his B.S. in Physics and Computer Science from Duke University in 1986, and his Ph.D. in Computer Science from the University of Illinois, Urbana, in 1991. After his studies, he worked for Motorola, Inc. in Austin, TX, where he was the manager of the High Performance Design Technology group. Since August 2001, he has been on the faculty at the University of Michigan, where he is a Professor. He has published over 450 papers and holds 40 patents. His work has focused on VLSI design, with particular emphasis on ultra-low-power and high-performance design. He was the Technical Program Chair and General Chair for the International Symposium on Low-Power Electronics and Design. He was also the Technical Program Co-Chair of the ACM/IEEE Design Automation Conference and a member of the ISSCC Technical Program Committee. He is an IEEE Fellow.

F5: *Advanced RF CMOS Transmitter Techniques*

Organizer: **Piet Wambacq,** imec, Leuven, Belgium

Committee: **Stefano Pellerano,** *Intel, Hillsboro, OR*
Sven Mattisson, *Ericsson, Lund, Sweden*
Shouhei Kousai, *Toshiba, Kawasaki, Japan*
Ali Afsahi, *Broadcom, San Diego, CA*
Taizo Yamawaki, *Hitachi, Tokyo, Japan*

Integrated transmitters for mobile applications face increasingly stringent specifications due to increasing modulation bandwidth and dynamic range for higher data-rates and reduced out-of-band emissions and noise for coexistence. Long battery life, low cost and small form factor require high efficiency and large integration levels.

On the other hand, the digital-analog boundary comes closer to the antenna. Further, new scaling-friendly paradigms are coming up, such as the use of switched capacitors in transmitters.

This forum presents the latest advancements in high-bandwidth, high-efficiency CMOS-based transmitter targeted for mobile devices, from both system architecture and building-block design perspective.

A Technical Foundation for RF CMOS Transmitters
Earl McCune, *RF Communications Consulting, San Francisco, CA*

RF power amplifier design is a century-old practice that still continues to evolve and progress today. Customer desires for linearity, output power, energy efficiency, and low cost are a mutually exclusive set of properties. Working through the resulting trade-offs for any particular design requires an excellent grounding in the physical fundamentals involved in these circuits. Ambiguities resulting from this long history (e.g. gain; knee voltage; envelope tracking) are resolved in a clear and physically consistent manner. There is not a perfect PA architecture, so a rapid survey of the major architectures sets the stage for further technical details. Fundamental challenges of CMOS PA design are pointed out. New results are presented for: true switching-PA design; physical interpretations of the linearity vs. energy efficiency trade-off; and operation details for the primary dynamic power supply (DPS) architectures of envelope tracking and direct polar modulation.

Earl McCune is a native of San Francisco and received his Bachelor's degree at UC Berkeley, his Master's degree at Stanford, and his Doctorate degree at UC Davis. His experience in RF circuits, signals, and systems extends over more than 40 years. Within this career he has founded two Silicon Valley startups, first doing modulated direct digital synthesis in 1986, which merged with Proxim in 1991. The second did switch-based RF transmitters from 1996 and was acquired by Panasonic 10 years later. He retired from Panasonic in 2008 as their only Technology Fellow from outside Japan. He currently has 69 issued patents in the USA. He is a multiple book author with Cambridge University Press for *Practical Digital Wireless Signals* and *Dynamic Power Supply Transmitters*, and is an IEEE MTT Distinguished Microwave Lecturer from 2013.

Cellular High-Power CMOS PA and SOI Switches
Kohei Onizuka, *Toshiba, Kawasaki, Japan*

Low-cost, easy-to-implement, silicon-based solutions for high-power RF frontend modules are essential for today's smart phones. Advances in both circuit and device technologies as well as synergistic enhancements to surpass performances of conventional compound semiconductor modules are highly demanded.

The first half of this talk describes recent progress in Watt-level CMOS PAs. Doherty and power supply control as circuit techniques improve back-off efficiencies critical to state-of-the-art WiFi systems, while Cu-plating and LDMOS as device technologies improve overall power efficiency and device reliability.

The second half of this talk demonstrates SOI-based solutions providing attractive functions to the system. Low-insertion-loss SOI switches not only replace conventional antenna switches but also enable automatic impedance tuning for TX power saving using a CMOS PA having impedance detection and control capability.

Kohei Onizuka received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2003, 2005, and 2008, respectively. Since 2008, he has been with the Corporate Research & Development Center, Toshiba Corporation, Kawasaki, Japan, where he was designing RF front-end circuits, power converters, and wireless power-transfer systems. Since 2013 he has been a visiting researcher at the MIT Medical Electronic Device Realization Center (MEDRC), where he conducts research in wearable health-care devices and medical diagnosis technologies based on ultrasound and optical spectroscopy.

RF Transmitters Must Byte the Digit
Ali Niknejad, *University of California, Berkeley, CA*

Transmitters for mobile applications now operate over wider channel bandwidths, utilize more complex modulation, and require operation in multiple bands. Designing efficient transmitters that can adapt to these needs is challenging. Spectral regrowth and spectral emissions must be controlled, which may require dozens of PAs and filters to meet specifications. Our goal is the design of a reconfigurable transmitter that exploits the advantages of modern CMOS technology, placing more burden on DSP. These so-called "digital transmitters" are highly reconfigurable and efficient, amenable to Polar and Cartesian architectures utilizing Class D/D-1 cores with higher peak efficiencies than Class-AB counterparts. Due to their generic nature, a PA can be easily targeted to different standards and frequency bands. Design challenges such as spectral emissions and quantization noise will be discussed in detail. Design examples from 2.4 GHz WiFi, LTE, and 60 GHz WiGig will be provided.

Ali M. Niknejad received the B.S.E.E. degree from UCLA and his Master's and Ph.D. degrees in electrical engineering from UC Berkeley. He is currently a professor in the EECS department at UC Berkeley and faculty director of the Berkeley Wireless Research Center (BWRC) and the BSIM Research Group. Professor Niknejad is the recipient of the 2012 ASEE Frederick Emmons Terman Award for his work related to electromagnetics and RF integrated circuits. He is also the co-recipient of the 2013 ISSCC Jack Kilby Award for his work on an efficient Quadrature Digital Spatial Modulator at 60 GHz, the 2010 Jack Kilby Award for Outstanding Student Paper for his work on a 90 GHz pulser for medical imaging, and the co-recipient of the Outstanding Technology Directions Paper at ISSCC 2004 for co-developing a modeling approach for devices up to 65 GHz.

Charge-Based Signal Processing for Wireless Transmitters
Jan Craninckx, *imec, Leuven, Belgium*

Wireless transmitters face the challenge of combining high power efficiency with even higher performance requirements, like linearity, noise and spurious content. The latter has often led to rather traditional analog-based direct upconversion architectures, that do achieve the required signal quality. Several digital transmit techniques try to match the performance, while offering other advantages like area, power consumption and CMOS scaling. In this talk an overview of those techniques will be given, followed

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by the introduction of a new transmit architecture. After decades of circuits based on signal processing in the voltage, current or time domain, we will propose charge as the new quantity that allows to combine the advantages of both analog- and digital-based architectures. Being easily combinable with scaled CMOS implementation, this technique offers excellent power efficiency and digital control together with out-of-band filtering for noise and spurs.

Jan Craninckx obtained his MS. and Ph.D. degrees in microelectronics *summa cum laude* from the KU Leuven in 1992 and 1997, on the design of low-phase-noise CMOS integrated VCOs and PLLs for frequency synthesis. From 1997 to 2002 he worked with Alcatel Microelectronics as a senior RF engineer on the integration of RF transceivers for GSM, DECT, Bluetooth and WLAN. In 2002 he joined IMEC (Leuven, Belgium), where he currently is the senior principal scientist responsible for RF, analog, mixed-signal and data-converter circuit design. His research focuses on the design of RF transceiver front-ends in nanoscale CMOS for software-defined radio (SDR) systems. Dr. Craninckx is an IEEE Fellow and has authored and co-authored more than 150 papers, book chapters, and patents. He was the chair of the SSCS Benelux chapter (2006-2011), SSCS Distinguished Lecturer (2012-2013) and is an Associate Editor of the JSSC.

Digital Operation of Base-Station PAs Enabled by Extended-Drain CMOS

Mustafa Acar, *NXP, Nijmegen, The Netherlands*

In next-generation cellular communication systems, the base station needs to be more flexible and must be able to operate across several frequency bands and different standards (2G, 3G, 4G, etc.). This task is especially challenging for the power amplifier (PA) stage, since high average efficiency is also required at high output power. This presentation will focus on NXP's novel switch-mode outphasing power amplifier concept, which promises to offer the required flexibility in power amplifiers by a more direct digital control of the PA using dedicated RF PA drivers that achieve a high breakdown voltage in 65nm CMOS by introduction of an extended-drain structure.

Mustafa Acar received the B.S. degree (with honors) from Middle East Technical University, Ankara, Turkey, in 2001, and both the M.S. degree (high honor) and the Ph.D. degree, in 2003 and 2011, respectively, from the University of Twente, Enschede, The Netherlands. Since 2007, Mustafa Acar has been working on advanced driver and PA systems at NXP Semiconductors. Currently, he is leading the switch-mode PA activity of NXP Semiconductors.

Digital Polar PAs Using Switched-Capacitor Circuits

Jeffrey Walling, *University of Utah, Salt Lake City, UT*

CMOS is ubiquitous for computation, and as such plays an ever-increasing role in our lives as we use computation to improve working efficiency. Increasing levels of integration have made it possible to embed analog and RF circuits with digital processing in integrated systems. The RF PA has been the exception to integration in CMOS, owing to relatively poor performance (e.g., peak P_{out} and PAE) when compared to other semiconductor technologies (e.g., III-V compounds and SiGe). In this talk the switched-capacitor PA (SCPA) is introduced. It leverages CMOS inherent strengths of fast switching and lithographic matching to yield a linear, efficient digital PA. Further, multiple-supply-modulation (Class-G) SCPAs are introduced. This architecture enhances power-backoff efficiency. Details of standard and Class-G SCPAs will follow. Comparisons will be made to supply-modulated PAs and other digital PAs. Finally, the talk concludes with discussion of future improvements to the SCPA architecture.

Jeffrey Walling received the B.S. degree from the University of South Florida, Tampa, in 2000, and the M.S. and Ph. D. degrees from the University of Washington, Seattle, in 2005 and 2008, respectively. He was employed at Motorola, Plantation, FL working in cellular handset development. He interned for Intel from 2006-2007, working on highly-digital transmitters and CMOS PAs and continued this research while a Postdoctoral Researcher at the University of Washington. He is currently an Assistant Professor in the ECE department at the University of Utah. His current research focuses on high-efficiency transmitter architectures and reconfigurable PA design. Dr. Walling has authored ~40 articles and holds two patents. He received the Best Paper Award at Mobicom 2012, the Yang Award for outstanding graduate research from the EE Department at the University of Washington in 2008, an Intel Predoctoral Fellowship in 2007-2008, and the Analog Devices Outstanding Student Designer Award in 2006.

Envelope Tracking Operation of CMOS PAs

Bumman Kim, *Postech, Pohang, Korea*

Envelope Tracking (ET) is a very hot research item and is being deployed in real handsets. The ET technique is well suited for Multimode Multiband (MMMB) operation since the MM is handled by the supply modulator and the MB by the PA, in a separate fashion. The supply modulator for the ET operation is an ideal Power-Management Integrated Circuit (PMIC) for PAs, enhancing overall TX performance. For the proper operation of the ET PA, several factors need to be considered. The first one is the envelope shaping to get the best performance from the ET PA. The time alignment between envelope and phase information should be accurate. The distortion characteristic of the ET PA should be understood and a proper linearization technique should be applied. The modulator efficiency should be high both at high and low power levels. Detailed design issues for the ET PA will be discussed, based on a CMOS linear PA.

Bumman Kim received the Ph.D. degree in Electrical Engineering from Carnegie Mellon University, Pittsburgh, PA. He joined the Central Research Laboratories, Texas Instruments Incorporated, where he was involved in the development of GaAs power FETs and MMICs. He developed the first millimeter-Wave MMIC and semiconductor-based oscillator operation over 100GHz. In 1989, he joined the Pohang University of Science and Technology (POSTECH), where he is a POSTECH Fellow. He is involved in device and circuit technology for RF integrated circuits (RFICs) and power amplifiers. His group reported Doherty amplifiers, which are the most popular power amplifiers for mobile communication systems. He has authored over 400 technical papers in international journals and conferences. He is a fellow of IEEE and IET. In 2008, he received the Kyung-Ahm Academic Award in Engineering. He is a member of the Korean Academy of Science.

Wideband Radio Base-Station Transmitter Trends

Mats Klingberg, *Ericsson, Stockholm, Sweden*

Radio Units in cellular radio base stations have been developed during the recent years to support ever-wider bandwidths and a higher number of carriers, while simultaneously consuming less power, with the aim of getting more capacity into a smaller unit. These general trends are likely to continue, emphasizing the need for more efficient power amplifiers in macro base stations. Other trends are higher-order MIMO amplifiers and smaller cells in heterogeneous networks to further increase capacity. We need to pack an increased number of transmitters into each unit, with potentially lower output power per amplifier, which means that the control circuitry and overhead is becoming more important for the overall efficiency. This also drives the need for higher integration to be able to continue shrinking the overall footprint of the unit.

Mats Klingberg received the M.Sc. degree from the Royal Institute of Technology, Stockholm, Sweden, in 2000. After this he joined Ericsson as a Research Engineer within the Generic Technologies group, focusing on efficiency enhancement techniques for multi-carrier and WCDMA Power Amplifiers. In 2008 he became Senior Specialist in the area of nonlinear modelling and currently works in the Digital Radio department with radio algorithms, particularly linearization, and their implementation architecture.

F6: *I/O Design at 25Gb/s and Beyond: Enabling the Future Communication Infrastructure for Big Data*

Organizer: **Ken Chang,** *Xilinx, San Jose, CA*

Chair: **Frank O'Mahony,** *Intel, Hillsboro, OR*

Committee: **Elad Alon,** *University of California, Berkeley, CA*
Hyeon-Min Bae, *KAIST, Daejeon, Korea*
Nicola Da Dalt, *Infineon, Germany*
Eric Fluhr, *IBM, Austin, TX*
Frank O'Mahony, *Intel, Hillsboro, OR*

The demand for ultra-high speed transceivers continues to rise exponentially due to the insatiable demand for high-throughput interconnect. Standards between 25 and 32Gb/s are rapidly approaching maturity, and available products and IPs at these rates are iterating to push down power while extending channel-loss recovery limits. Predictably, specifications are now in early stages for extending per-lane bandwith to between 40 and 64Gb/s. Meeting these 25Gb/s+ targets, especially for long-reach applications, is stressing the capabilities of both the underlying circuitry and the communication channels, and has caused significant rethinking of the overall system and circuit architectures for these links. In particular, the debate about multi-level (PAM4) versus binary (PAM2) signaling and which path offers the best energy-efficiency/data-rate scalability has returned to the foreground. Similarly, the emergence of high-speed ADCs with sufficient resolution for link applications has driven renewed interest in DSP-based approaches, while other efforts have pushed more analog/mixed-signal link components to over 60Gb/s/lane. To further ensure low BER operations, sophisticated coding such as FEC is brought into the discussion. Even in the domain of optical communications, significant challenges related to the bandwidth capabilities of the optical devices as well as the back end processing are currently being addressed. In fact, some of the highest speed optical links are limited by the short electrical interconnect between the driver circuitry and the optical module itself. This forum presents state-of-the-art I/O techniques enabling such high line rates across both optical and electrical interfaces as well as a number of emerging standards such as 802.3bj, various flavors of CEI, and HMC (hybrid memory cube).

Challenges and Solutions for Next-Generation 40 to 56Gb/s Transceivers
Adam Healey, *Avago Technologies, San Jose, CA*
Industry standards for transceivers operating from 20 to 28Gb/s have been established and technology deployments are underway. Now the industry is turning its attention to next-generation transceivers operating from 40 to 56Gb/s. This next doubling of the data rate will amplify the challenges faced by the previous generation to deliver energy efficient links that operate over channels whose signal integrity lags the demand for bandwidth. This presentation will review possible applications of 40 to 56Gb/s transceivers, consider the challenges presented by these applications, and discuss solutions that industry standards and technology developers may consider to address them.

Adam Healey is a Distinguished Engineer at Avago Technologies where he contributes to the definition of high-speed transceiver architecture and the modeling of high-speed links. He contributes to industry standards through his work in the IEEE 802.3 Ethernet working group and the INCITS T11 Fibre Channel technical committee. He served as chair of the IEEE P802.3ap Task Force chartered to develop the standard for Ethernet operation over electrical backplanes at speeds of 1 and 10Gb/s. He also served as chair of the IEEE P802.3bj Task Force which defined 100Gb/s operation over electrical backplanes and cables and extended Energy Efficient Ethernet to 40 and 100Gb/s networks. He currently serves as the vice chair of the IEEE 802.3 Ethernet working group. He received BS and MS degrees in electrical engineering from the University of New Hampshire.

Link Modeling and Design at 40Gb/s and Beyond
Bryan Casper, *Intel, Hillsboro, OR*
A system level approach to design and manufacture future high-speed wireline links is necessary to optimize performance, cost, power and channel reach capability. Candidate architectures to exceed 40Gb/s electrical signaling rates are proposed and evaluated. System level tradeoffs are explored including channel topology and elements, process technology, equalizers, modulation, error correction and clocking. I will also demonstrate these tradeoffs using new methods that fully emulate I/O systems to achieve high confidence in the architectural and circuit analysis.

Bryan Casper is the Director of the Signaling Research Lab and Senior Principal Engineer with Intel Labs, based in Hillsboro, Oregon. He leads Intel's high-speed signaling research group responsible for the development and design of next generation high-speed mixed signal circuits and I/O systems. In 1998, he joined the Performance Microprocessor Division of Intel Corporation and contributed to the development of the Intel Pentium and Xeon processors. Since 2000, he has been a circuit researcher, contributing to the development of I/O self-test technology, signaling analysis methods, high-speed I/O circuit architectures and multiple I/O standards.

56Gb/s SerDes Transceiver Design: NRZ, PAM4, and Others
Jri Lee, *National Taiwan University, Taipei, Taiwan*
Next generation's electrical and optical data links necessitate transceivers operating at even higher data rates. In the field of 50+Gb/s, designers and engineers face severe trade-offs among technology nodes, cost, bandwidth limitation, compatibility to existing components, and power consumption. Testing environments and standards must be established as well. The existing 28Gb/s solution can be effectively extended to form a new solution for 56Gb/s. It can be done by either enlarging the available bandwidth with more advanced technologies (e.g., 16nm CMOS), or transforming the data format into PAM4. The speaker provides system and circuit level analysis on these trade-offs for 56Gb/s SerDes in advanced CMOS technologies. Both NRZ and PAM4 transceivers are introduced with silicon-proven measurement results. Specifications for 56Gb/s SerDes and roadmap for future development will be provided as well.

Jri Lee received the B.Sc. degree in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Los Angeles (UCLA), both in 2003. He joined National Taiwan University (NTU) in 2004, where he is currently a Professor of electrical engineering. Professor Lee received the Beatrice Winner Award at the 2007 ISSCC, the Takuo Sugano Award at the 2008 ISSCC, the Author-Recognition Award at 2013 ISSCC, and other international and domestic awards. He also received the NTU Outstanding Teaching Award in 2007, 2008, and 2009. He has served on the Technical Program Committees of ISSCC from 2007 to 2010, and the Symposium on VLSI Circuits (2008~present). He was a guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2008. He served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society from 2011 to 2013.

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ADC-and-DAC-Based Transceivers for 100Gb Ethernet
Jun Cao, *Broadcom, Irvine, CA*
New Ethernet standards, such as 802.3bj, respond to the need for higher data rates over backplanes and copper cables to reach 100Gb/s throughput. ADC-DAC-based transceivers enable advanced signal modulation and integrated DSP to combat channel impairments. Interleaved structure propels ADCs to higher speed while the mismatch calibration is the key to achieve better ENOB. Choice of sub-ADCs has a direct impact on the system performance such as power, latency and BER. While flash ADCs dominate 10GE applications, SAR ADCs are more widely used for 100GE. High-speed DAC is essential for modulation formats such as PAMx and provides precise multi-tap FIR for the transmitter. DACs at speeds higher than 10GS/s are discussed and their application in PAM4 signaling is demonstrated, including a DAC integrated in a 802.3bj-compatible-transceiver that enables 36Gb/s transmission over legacy low bandwidth channels.

Jun Cao (S'96-M'99-SM'14) received the B.S. degree in physics from Peking University in 1994, MSEE from the University of Michigan in 1996 and the Ph.D. degree in electrical engineering from UC Irvine in 2003. In 1999, he joined NewPort Communications as one of the leading designers for the world's first commercial 10G CMOS transceiver. Since 2000, he is with Broadcom's analog group, currently as a senior manager and a distinguished engineer. He has published more than 30 journal/conference papers, with more than 20 in ISSCC/JSSC, on the topic of high speed transceivers and data converters. He also has more than 50 U.S. patents.

Low-Power CMOS ADCs for 100+Gb/s Wireline Communications
Lukas Kull, *IBM Research, Zurich, Switzerland*
Next-generation high-speed communication systems implement more complex signaling to achieve better bandwidth efficiency and higher data rates. Key components for these systems are low-power high-speed CMOS ADCs, which enable the integration of the entire system (ADCs and DSP) on a single chip. Recently, interleaved SAR ADCs were shown to be an excellent solution to provide both high speed and low power consumption. Several design techniques for low-power interleaved SAR ADCs suitable for 100Gb/s communication systems are presented. Future trends and limitations of key figures for high-speed CMOS ADCs based on current hardware and latest CMOS technology will be highlighted.

Lukas Kull received the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology, Zurich (ETH), Switzerland, in 2007 and the Ph.D. degree from the Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland, in 2014.He joined IBM Research – Zurich, Rüschlikon, Switzerland, in 2010, where he has been involved in analog circuit design for high-speed low-power ADCs. His research interests include analog circuit design, IR and THz imaging. In these areas he authored or co-authored more than 20 patents and technical publications.

Digital Signal Processing Chips for 100-to-400Gb/s Optical Communications
Oscar Agazzi, *Clariphy Communications, Irvine, CA*
Advanced DSP finds widespread use in current and future optical communications. Long haul and submarine links at rates of 100Gb/s and beyond have made a transition to coherent modulation and high spectral efficiency modulation formats. Per-wavelength data rates of 200Gb/s using DP-QAM16 are currently starting to be deployed. DSP and advanced modulation and coding also find application in shorter reach links such as inter and intra data center communications, with maximum lengths ranging from a few hundred meters to about 100km. This presentation will discuss next-generation transceivers for applications ranging from intra data center to submarine links and the ways they will impact optical communication networks.

Oscar Agazzi is the Senior Vice President and Chief Systems Architect at ClariPhy Communications,. He is the chief architect of the ClariPhy family of coherent as well as direct detection optical transceivers. Prior to joining ClariPhy, he worked at Broadcom and at Lucent Technologies Bell Laboratories. Dr. Agazzi holds a Ph.D. in Electronic Engineering from the University of California at Berkeley. He has over 150 patents issued or pending, and has published more than 60 technical papers in journals and conferences. He is a Lucent Technologies Bell Labs Fellow and a Fellow of the IEEE.

Analog/Mixed Signal Designs for Over-25Gb/s Server Links
Hirotaka Tamura, *Fujitsu Laboratory, Kawasaki, Japan*
The bandwidth of inter- and intra-server links needs to be increased to over 25Gb/s/lane while keeping the power consumption and circuit area within a tight budget. This talk describes analog and mixed-signal transceiver designs for such high-speed server links, focusing on comparator designs and power reduction means like baud-rate sampling. I also look at high-speed DFE implementation, blind-clock phase recovery schemes, and CDR designs for multi-lane repeaters using different phase-adjusting circuits.

Hirotaka Tamura received his B.S., M.S., and Ph.D. degrees in electronic engineering from Tokyo University, Tokyo, Japan, in 1977, 1979, and 1982. He joined Fujitsu Laboratories in 1982. After being involved in the development of different exploratory devices such as Josephson junction devices and high-temperature superconductor devices, he moved into the field of CMOS high-speed signaling in 1996 and got involved in the development of a multi-channel high-speed I/O for server interconnects. Since then he has been working in the area of architecture- and transistor-level design for CMOS high-speed signaling circuits. He is a Fellow of the IEEE.

Power-Efficient Design Approaches for >60Gb/s Transceivers
Chih-Kong Ken Yang, *University of California, Los Angeles,* CA
In the design of high-speed SerDes links, power is a serious consideration especially as the signaling frequency is a substantial fraction of the f_T of the underlying CMOS technology. Power drain is even more severe when dealing with lossy channel characteristics. This talk discusses on the implementation challenges of pushing data rates toward 60+Gb/s across relatively short and clean channels but still with moderate attenuation (20 to 30dB loss at the Nyquist frequency). In particular, the talk focusses on recent circuit design approaches and innovative circuit architectures that can lead to good power-performance tradeoff in implementing key circuit elements such as the serialization, clocking elements, and transmit and receive equalization.

Chih-Kong Ken Yang (S'94-M'98-SM'07-F'10) was born in Taipei, Taiwan. He received the B.S. and M.S. degrees in 1992 and the Ph.D. degree in 1998 from Stanford University, Stanford, CA in electrical engineering. He joined University of California at Los Angeles in 1999 and has been a Professor since 2009. His current research area is high-performance mixed-mode circuit design for VLSI systems. Research interests include clock generation, high-performance signaling, low-power digital functional blocks, analog-to-digital conversion, high-voltage generation, and networking. He is a fellow of the IEEE.

ES1: Student Research Preview

Chair: Jan Van der Spiegel,
University of Pennsylvania, PA

Co-Chairs: ***SeongHwan Cho***
Marian Verhelst

Session 1: Low-Power Data Converters and High-Speed Links

Chairs: Denis Daly, Andrea Baschirotto

Wenjuan Guo	*University of Texas at Austin, USA*
Zhijie Chen	*Tokyo Institute of Technology, Japan*
Jianyu Zhong	*University of Macau, China*
Claudio De Berti	*University of Pavia, Italy*
Yingyan Lin	*University of Illinois at Urbana-Champaign, USA*
Ke Huang	*Tsinghua University, China*
Shuai Yuan	*Tsinghua University, China*

Session 2: Biomedical Circuits and Systems

Chairs: Tinoosh Mohsenin, GuoXing Wang

Ka-Meng Lei	*University of Macau, China*
Hongjie Zhu	*University of Pennsylvania, USA*
Wala Saadeh	*Masdar Institute of Science and Technology, UAE*
Hsin-Chih Kuo	*National Cheng Kung University, Taiwan*
Hugo Cruz	*National Cheng Kung University, Taiwan*
Shunli Ma	*Fudan University, China*
Kok-Hin Teng	*National University of Singapore, Singapore*
Shahab Shahdoost	*Case Western Reserve University, USA*
Zhibin Xiao	*Fudan University, China*

Session 3: Energy-Efficient Circuits for Sensors, RF, and Platform

Chairs: Patrick Reynaert, Jeffrey Weldon

Saleh Masoodian	*Dartmouth College, USA*
Sungrok Jeon	*KAIST, Korea*
Joonseok Yang	*Seoul National University, Korea*
Xu Meng	*National University of Singapore, Singapore*
Shih-En Chen	*National Cheng Kung University, Taiwan*
Yiming Yu	*University of Electronic Science and Technology of China, China*
Antonio Pullini	*ETH Zürich, Switzerland*
Suma George	*Georgia Institute of Technology, USA*
Viveka Konandur Rajanna	*Indian Insititute of Science, Bangalore, India*

Poster Session

Session Chairs: Vincent Gaudet and Dejan Markovic

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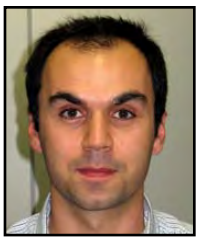
ES2: Brain-Machine Interfaces: Integrated Circuits Talking to Neurons



Organizer: **Firat Yazicioglu,** *IMEC, Leuven, Belgium*
Peng Cong, *Google, Mountain View, CA*
Shahriar Mirabbasi, *University of British Columbia, Vancouver, Canada*

Chair: **Peng Cong,** *Google, Mountain View, CA*
Shahriar Mirabbasi, *University of British Columbia, Vancouver, Canada*

"We have not unlocked the three pounds of matter sitting in between our ears," said Barack Obama. The brain is the most complex human organ, with energy efficiency far beyond that of any existing equivalent computing technology. Great efforts are being invested globally into deciphering its functioning. If successful, the resulting knowledge may forever change medical, consumer, and communications semiconductor industry sectors.

A first significant challenge on the road towards this goal is the creation of instruments, generally enabled by integrated circuits, which can interact with a large number of the brain neurons and interpret such interactions.

This evening session will discuss technologies and circuit design solutions for connecting integrated circuits to neural circuits, and will explore future application opportunities for such brain-machine interfaces. Experts in related technologies, circuit design, and applications from three continents will present an entertaining session on the impact of semiconductor technologies on medical applications and human-machine interaction.

Panelist's Statements

Neural Interfacing: Challenges and Opportunities for Circuit Designers

Tim Denison, *Medtronic, Minneapolis, MN*

The burden of neurological disease represents a large unmet need with significant societal and economic impact. While promising in-roads for treatment have been made for some conditions, the application of medical technology to address the broader space of neurological disorders is often limited by the lack of suitable technology and by scientific unknowns. Technologists are helping to address these issues by creating translational research tools, permitting the chronic probing of diseased circuits, as well as developing new interface approaches with improved reliability. The hope is that clinicians, scientists and engineers can jointly develop therapeutic concepts from first-principles. To help make these systems practical, several constraints must be considered, including balancing the risks and benefits of the system from the patient's perspective. This talk will provide an overview of the state of the art in neural technology, and use this to highlight the remaining challenges and opportunities from the perspective of a circuit designer.

CMOS Technology to Interface with Single Neurons and Axons

Andreas Hierlemann, *ETHZ, Zurich, Switzerland*

CMOS technology constitutes an enabling technology to batch-produce high-density microelectrode arrays (HDMEAs) with thousands of micro-scale electrodes. The resulting complex microsystems feature, on the very same chip, electrode-addressing logic, signal-conditioning circuitry units that provide excellent signal-to-noise characteristics, as well as stimulation units, A/D conversion and a digital interface. These microelectrode arrays can be used for biomedical and fundamental *in vitro* neuroscience research and provide extracellular electrophysiological information at high spatio-temporal resolution down to the level of single cells or single axons. The utility of CMOS HDMEAs with more than 3000 electrodes per mm^2 for electrophysiological analysis of signals of neurons or networks of neurons in dissociated or organotypic cultures and acute tissue slices will be demonstrated. In all cases, many electrodes can be simultaneously used to record from the same neuron or axon.

Circuits and Systems for Implantable Brain Monitoring

Jan Rabaey, *University of California, Berkeley, CA*

Acquiring deeper insights into the dynamic behavior of the brain requires imaging capabilities operating at multiple scales of resolution – from microns to the complete brain. Recent advances in microscopic sensing, ultra low-power mixed-signal processing and communications lead to interfaces that may be able to observe and modulate thousands of active neurons *in vivo* at different locations in the brain. This will open the door for viable long-term brain-machine interfaces that restore function for people with severe neural disabilities. However, accomplishing this goes beyond realizing the pure neural interfaces. It requires an integrated system solution that includes extracting relevant parameters from the observed data volume (which is huge and noisy), and employing those in a real-time closed-loop control setting with bounded latency, translating into sizable computational requirements.

Neural Stimulation and Closed-Loop Prosthetics

Minkyu Je, *Daegu Gyeongbuk Institute of Science & Technology, Daegu, Korea*

Neural stimulation has been widely used as an effective treatment in medical devices such as pacemakers, deep-brain stimulators, retinal/cochlear implants, and functional electrical stimulators. To enable the eventual realization of closed-loop prosthetics, bidirectional interfaces between integrated circuits and neural circuits are necessary, where neural stimulation passes information from the integrated circuits to the neural circuits, and neural recording is used in the other direction. For successful implementation of the neural stimulation function, several important factors such as stimulation efficacy, human safety, and energy efficiency need to be considered. In addition, when implemented along with the recording function for closed-loop prosthetics, special attention needs to be paid on mitigating the problems caused by stimulation artifacts. In this talk, the circuit techniques developed to address such factors are presented, as well as a closed-loop peripheral nerve prosthetic device being developed to restore limb functions is introduced.

EP1: Moore's Law Challenges Below 10nm: Technology, Design and Economic Implications




Organizers: **Bing Sheu,** *TSMC, Hsinchu, Taiwan*
Kathy Wilcox, *AMD, Boxborough, MA*
Ali Keshavarzi, *Cypress, San Jose, CA*

Moderator: **Dimitri Antoniadis**, *MIT, Cambridge, MA*

Moore's Law has governed advances of silicon technology for more than four decades, providing a tremendous reduction in cost per transistor. Device geometry, packing density, speed performance, and manufacturing cost of a single transistor have scaled together –according to Dennard scaling rule. Approaching the sub-10nm era and beyond, Moore's Law faces serious challenges in the near future (5-6 years). Device geometry/density/performance/cost will not scale simultaneously anymore. What are the new scaling rules for logic and memory? Researchers are racing to address 3 scenarios: 1) extending silicon, 2) beyond silicon, and 3) beyond CMOS.

What is the impact of future scaling trends on semiconductor technology and design? How will the industry continue to attract the hundreds of billions of dollars of investment necessary to continue the pace of scaling we have been accustomed to, and also attract young talent to the semiconductor industry? Will 2.5D/3D integration and system innovations come to the rescue? How do we continue to scale power efficiently? How do we manage cost and economic considerations going forward?

Panelist's Statements

Mark Bohr, *Intel, Hillsboro, OR*
Our industry has reaped the benefits of Moore's Law for 50 years now, making integrated circuits that have grown from tens to billions of transistors and performing an increased range of functions from memory to logic to signal processing. Scaled transistors have provided significant improvements in performance and low power, but the main benefit of scaling has been lower cost per transistor. As we scale to 10nm and below, it is becoming increasingly difficult to achieve traditional improvements in performance, power and cost due to inherent leakage and resistance increases of scaled devices, and the increased cost of added masking layers. Moore's Law can continue beyond 10nm by developing new materials and device structures to meet performance and power requirements, and by close collaboration between process development and product design teams to ensure that the right features are chosen to deliver both improved density and lower cost per transistor.

Jack Sun, *TSMC, Hsinchu, Taiwan*
Despite the recent challenges of escalating wafer manufacturing cost due to patterning complexity and the introduction of new materials and transistor structures, there are many opportunities to continue cost-per-function scaling. Past challenges in Moore's Law have been overcome through innovations in monolithic technology (Cu/low-k, strain, high-k/metal gate, FinFET, immersion lithography), chip design (new circuits, power management), and system architecture (parallelism, multi-/many-core, better processor architectures). Going forward, we must take a holistic approach to scaling, i.e. energy-efficient system scaling or superchip scaling with "3D×3D" for system miniaturization to enable new products and applications through collaborative innovation in an open platform and symbiotic ecosystem. 3D transistors, 3D memory cells, and 3D integration or stacking of logic, memory, and specialty function chips are examples of 3D×3D to increase transistor count and function per footprint, as well as to reduce system form factor and interconnect overhead. It is also time to explore new switches and architectures, e.g. Si-based neuromorphic computing to achieve the energy efficiency of biological systems.

Liam Madden, *Xilinx, San Jose, CA*
Happy 50th birthday Moore's Law! In reflecting on the last 50 years, one is tempted to say that given a very powerful hammer the industry has seen only nails. Unfortunately that hammer (area scaling) is now finding fewer and fewer nail like objects to hit and the cost of swinging the hammer is getting more and more expensive. Happily there is another tool in the engineer's toolbox that can give much better results. While the hammer crowd wait (and wait and wait) for EUV to pop up a few more nails to whack, enterprising craftsmen and women are using 3D stacking to address a range of challenges from defect-based cost constraints to interchip signaling at unparalleled power/performance levels. On the 40th anniversary of Moore's Law, Gordon famously said: "Moore's law is really about economics". The "dismal science" is clear on chip scaling. The days of the hammer are numbered but the promise of cost reduction continues for those that are just willing to check their toolbox.

Mark Hill, *University of Wisconsin, Madison, WI*
Mark will share perspectives on the future of computer architecture in response to application opportunities and semiconductor challenges. In particular, from a community white paper he led called "21st Century Computer Architecture", he will discuss how future computer architecture must consider context – from sensors to data centers, energy efficiency beyond parallelization to specialization, responses to new technologies, and design options that cross-cut traditional computer system layers.

Geoffrey Yeap, *Qualcomm, San Diego, CA*
The key FOM of (speed×density)/power/cost for traditional Moore's Law scaling has slowed down after the 28nm technology node. Die size scaling post the 28nm node has faced process cost challenges (e.g. complexity of double patterning and local interconnect). System scaling should continue through orthogonal 2.5D/3D system-in-package scaling and architecture-design-technology co-design along with innovations in transistor architecture and local/global interconnects to preserve Moore's Law. The singular focus on increasing the number of logic transistors per unit area must shift to maximizing the value using the minimum number of lowest cost transistors. The end user's value is market and application specific. For mobility applications, the percentage of CPU silicon area has decreased, while silicon area for visual/audio computing (GPU, image signal processor), communication (4G-LTA-A, WiFi), RF front-end and sensory functions has increased. I will discuss these issues from a fabless and an application/market-driven perspective on how we should proceed, while considering the impact on the technology and design.

Jo De Boeck, *imec, Heverlee, Belgium*
The harder it gets to predict what the next-next "node" will be like, the more interesting the research challenges become. Various device options and routes for integration and interconnect from decades ago may enter the scene. To stay in sync, revisit your textbooks for III-V, tunneling, vertical geometry, quantum effects, spin, optical functions and smart interposers. These concepts are all on the design table today. The impact at the circuit and system level (cost, performance, power) of the above options is key for our industry ecosystem. It guides decisions on market opportunities and economics at play, where application insights are invaluable. Moving fast in screening options, while collaborating across disciplines and innovation actors, is required to stay on track of whatever economic scaling law we'll end up implementing. During the ISSCC evening panel, I will elaborate more on these latter aspects.

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EP2: Lost Art? Analog Tricks and Techniques from the Masters



Organizer: **Tsung-Hsien Lin,** *National Taiwan University, Taipei, Taiwan*
Carlo Samori, *Politecnico di Milano, Milano, Italy*
Richard Schreier, *Analog Devices, Toronto, Canada*

Moderator: **Richard Schreier,** *Analog Devices, Toronto, Canada*

Analog design has sunk into a local minimum characterized by tired old topologies and well-worn design techniques. This panel will shake things up with a combination of circuit gems and design methodologies mined from the brains of some of our community's most creative individuals. Prof. Asad Abidi will explain the operation of a common yet often inadequately understood circuit containing just a single FET. Barrie Gilbert will then amaze you with a collection of translinear circuits exploiting the mighty BJT. Jan Craninckx will take a different tack, showing that true magic is possible nowadays with digitally-assisted analog design, in which calibration blocks form the basic units of creativity. Professors Shoji Kawahito and Rinaldo Castello will return to straight circuits, showing gems used in imaging ICs and power-efficient rail-to-rail amplifiers. Lastly, Prof. Huei Wang will bring the discussion back to design techniques by asking if traditional RF design is a Lost Art, perhaps deservedly so.

Panelist's Statements

Asad Abidi, *University of California Los Angeles, Los Angeles, CA*
How many ways can one use a FET-R-C loop? In more ways than one might imagine. Switching the FET periodically, it is a sample-and-hold. Switching at a low duty cycle, it is the front-end of a sampling oscilloscope. Switching synchronously with a carrier frequency, it is a downconversion mixer. Multiple FET-C branches operating at uniformly spaced clock phases will deliver the modulation as a vector in the complex plane. What is the gain of this circuit? What is its frequency response? What is its noise figure? The circuit may be simple, but not so the answers.

Barrie Gilbert, *Analog Devices, Portland, OR*
Way back in the annals of analog IC history, using those oft-forgotten toys called Beejay-tease, the Translinear Principle made its appearance. At first, no one knew what to make of it – or what to make with it. Looking back on its discovery nearly fifty years ago, elders of the analog persuasion now wonder how they could have done without it. The ubiquity of TL circuits is now well established, although it may not always be clear to a modern designer that in fact the pervasive value of "translinearity" is being invoked in common circuit topologies. We will look at just a few of the acts on display at this circus, well aware that many sitting around the ring, weaned on dried moss, will be filled with envy, and probably rush out to buy a good book on bipolar analog design.

Jan Craninckx, *IMEC, Leuven, Belgium*
I truly enjoy the beauty and elegance that is present in many refined analog circuits, I'm often amazed by the innovation and intelligence that analog designers can put in the realizations. "Art" is the correct terminology for this.

But that should not stop us from being pragmatic if possible. Many of these circuits are in the end still limited by some fundamental laws dictated by Mother Nature that cannot go beyond the typical power/noise/linearity trade-offs we encounter every day. Many systems in the last decade have proven that with the right amount of digital, it is possible to correct mismatch, it is possible to compensate nonlinearities, it is possible to keep performance over PVT variations, etc. If the overall system cost can be lowered by employing these techniques, we should use them.

Shoji Kawahito, *Shizuoka University, Shizuoka, Japan*
In circuits used in an array-structured device as in column analog circuits for CMOS imagers, high performance must be maintained under extremely severe constraints and conditions. The circuits must be embedded in a micrometer-pitch column and work elegantly while receiving interferences from other columns. Column-parallel analog-to-digital converters (ADCs) have become a key technology for CMOS imagers. The resolution of 14b or more, dynamic range of 80dB or more and offset error of almost zero are required. In 8K4K imagers, for instance, 8,000 ADCs work in parallel and must have equal performance. The pitch of the column-parallel ADC is a few micrometers and the delicate image signal must be maintained during the A/D conversion without interference from the adjacent columns and clock signal lines which run quite closely to the sensitive analog circuit part of the ADC. The solution to these problems, while meeting the performance required for high-spec imagers, is often provided by circuits with less than two-dozen transistors. Circuits with two-dozen transistors will still provide great impact on the future development of CMOS imagers for various applications including biomedical, industrial, automobile, and consumer products.

Rinaldo Castello, *University of Pavia, Pavia, Italy*
Amplifiers capable to drive small resistors and/or large capacitors over a large bandwidth are key building blocks of mixed signal chips. Ensuring high linearity with the highest power efficiency is difficult to achieve. The task becomes even more challenging when an output swing that approaches the supply rails is demanded. In this situation the class A/B output stage becomes critical to achieve the target performance. The two key goals of any push-pull designer are: First, rail-to-rail driving capability of the complementary common source output transistor with precise control of their quiescent current level. Second, robust frequency compensation that ensures stable response for a low and significantly varying impedance load. A compact circuit that simultaneously address both of the above points in a very elegant way is extremely useful and deserve to be discussed. Achieving this goal with a small number of transistors is even more challenging.

Huei Wang, *National Taiwan University, Taipei, Taiwan*
As silicon-based device technologies advanced quickly, RFICs in the microwave/millimeter-wave regime are somewhat like analogue circuits nowadays. Many designers with an analogue circuit background tried to design microwave, and even millimeter-wave RFICs, using the skills which they learned from analogue circuit design classes, and achieved some successful circuit performance. Conventional design techniques, such as impedance matching and the concept of distributed elements for microwave circuit design, seem to have become the "lost art". However, is it really enough for us to simply utilize analogue circuit design techniques for millimeter-wave RFIC design? Can all of them be applied in the design? On the other hand, is a conventional microwave circuit design approach really necessary? It might be interesting to debate whether the "lost art" is indeed lost or not.

EP3: Innovating on the Tapeout Treadmill


Organizer: **Jack Kenney,** *Analog Devices, Somerset, NJ*
Frank O'Mahony, *Intel, Hillsboro, OR*

Moderator: **Jack Kenney,** *Analog Devices, Somerset, NJ*

In your current job, would you describe yourself as a "Brilliant Technology Innovator" or "Indentured Spice Monkey"? In the competitive and fast-paced semiconductor industry, most jobs require people to do at least a little (but more often a lot) of both. And your answer may change on a daily or hourly basis. But how do corporations, universities and the technologists at the heart of these organizations strike the right balance between blue-sky innovation and disciplined execution? What priorities and policies distinguish the industry leaders from the industry followers?

Fundamentally the answers to these questions depend on how risks and rewards are managed. On the one hand, the semiconductor industry is highly competitive, and missteps in product execution and research can significantly impact revenue stream and funding. A conservative strategy is to make minor increments on existing designs in order to guarantee performance with aggressive delivery dates. However, IC companies must find ways to differentiate their products, or they risk being stuck in commodity markets with little opportunity for revenue and profit growth. In addition, over the long term engineers who find themselves in a frantic, high-pressure race toward mediocrity can get burned out and become less effective or leave. Being a successful innovator requires taking risks. The question we pose is: "How do IC companies encourage innovation while meeting tight product development schedules?"

In this panel discussion, seasoned experts from both corporations and academia explore how innovation is best planned, executed and prioritized.

Panelist's Statements

Uming Ko, *MediaTek, Austin, TX*
Needless to say, there is a strong correlation between an organization's growth and its innovation pace, especially in high-tech industries. While broader innovation can best be fostered in a "white-space" R&D organization, in and of itself can be hard to justify if decoupled from product development. On the other hand, a traditional, "operation-focus" execution can yield "me too" products and easily sap employee morale, hence not sustainable. Acknowledging the dilemma, either a new paradigm will have to be embraced or be dinosaured out. So, we might as well welcome this new age of "inno-cution" where innovations must be injected at a fast-pace, risk-mitigated product execution, or face being displaced by the ones who can.

The concept is not new at all, as similar paradigm shifts have occurred in the past. For instance, automotive innovation is happening at a much faster pace today than in any time during the past few decades, creating hybrid and EV vehicles, and soon the user-friendly smart-car. An extreme example is smartphone innovation, initiated by the iPhone introducing the touch-screen to replace the keyboard, followed by larger screen sizes to support higher screen resolutions and simplifying user-input, then the disruptive, high cost-performance (CP) valued innovations by MediaTek making it affordable for everyone. "Everyday Genius" has been one of the key elements to make disruptive innovation possible, and will continue to drive MediaTek's "inno-cution" in moving forward!

Chris Mangelsdorf, *Analog Devices, San Diego, CA*
The hamster is one of the most delightful, contented creatures you'll ever meet. But take away its exercise wheel and what've you got: a rat without a tail. The tapeout treadmill is the engineer's exercise wheel. Without it, without a goal, the engineer becomes about as useful as a dipstick on a Tesla. Necessity is the mother of invention. Take away necessity and invention becomes an orphan: the results are bizarre solutions in search of a problem. So you can't stop the treadmill in the hopes of inspiring a breakthrough. Likewise, you can't "set aside" time for invention, because forcing yourself to be creative is like forcing yourself to sleep. It doesn't work. The harder you try the less you succeed. My advice is to take a lesson from our small furry friends and learn to love the treadmill. If you've got a problem, blame the hamster, not the wheel.

Michael Neuhauser, *Infineon Technologies, Neubiberg, Germany*
It's all about people, culture and the consistent use of professional management tools. An R&D organization which is in a permanent overload situation will create over time more and more mistakes and quality issues, which results in a further overloading of the teams. This kind of downward spiral is eating up the energy and creativity of each engineer over time and the room to create innovation is gone. The risk is high that the teams will burn out and at the same time the execution quality and the innovation capability of an organization is going down significantly. In addition if this is done in an environment of fear where mistakes are punished immediately, the willingness to take risky innovative approaches will drop. To overcome this well- known problem we are using different tools like pipeline management to measure and plan the workload of our R&D teams properly and giving them room for innovation. Within the Infineon High Performance Behavior Model two of the eight shared values of our organization are "Drive value through innovation" and "Be ambitious and manage risks". We have built processes, methods and motivation measures to implement these values and to avoid the classical downward spiral.

Jinho Park, *Terasquare, Seoul, Korea*
The semiconductor sector is becoming more commoditized, and in the future, mergers among companies will accelerate consolidation of the industry. This will result in size expansion of semiconductor companies, and amidst competition among large scale semiconductor companies, the generation and growth of venture semiconductor companies shall be increasingly challenged. In such circumstances, for small and medium companies to survive, the development of new products through cost and time-efficient innovation becomes essential.

One method of achieving this is cooperating with academia: academia can assume initial research, which entails risk in terms of cost and time, while the company focuses on product development, which is directly linked to production and sale. However, in this case, there exist trade-offs involving the distribution of IP ownership and licenses, distribution of profits arising from sale of products, division of labor, and security issues. For tie-ups between academia and companies to be actually effective, good examples must be produced through the passage of time.

Liesbet Van der Perre, *IMEC, Heverlee, Belgium*
"Fly with the eagles" when it comes to innovation, it is a key aspiration of R&D groups and industry leaders. To support the explosive growth in mobile data and connected devices beyond 2020, chip solutions with substantially better performance-power ratio are needed. Incremental optimizations of current designs will not do. Exploiting new technologies (e.g., FinFETs) and re-thinking circuits and architectures is unavoidable. We put in place our IMEC-flavor of 'time boxes', a stage-gated process tailored for high-potential high-risk R&D. It challenges inventive teams of designers and device/process experts to take time to imagine and discover beyond the known and proven concepts. Time and resources are 'boxed' and progress assessed regularly. The aim is to benchmark, defining bold targets and delivering timely. The result can be a clear plan for a full-blown research track or a clear scientifically sound opinion of why certain options are better left untouched (for now). In the rush for industrially relevant results with short term impact, this process encourages creativity and points to unforeseen routes.

Myles Wakayama, *Broadcom, Irvine, CA*
Innovation happens. It happens because engineers have the burning need to create, to find better solutions to any and all problems before them. This is why they become engineers in the first place and goes well beyond their day jobs. Innovation happens anywhere and at any time. The best ideas often come during unglorified situations of unbearable duress well past midnight, in a laboratory seeking a minimally invasive solution to restore your biggest customer's production lines, or go out of business. It is true that innovation happens during leisurely moments at the local coffee shop, but such moments are an unnecessary luxury for great innovation to happen. Innovation succeeds when decision makers are highly technical, and trust the creative talents of their engineers. The decision makers guide and filter for relevance and quality, and prioritize and promote the best innovation of their engineers. Without that your engineers become disgruntled, and the dreaded tapeout treadmill begins. Treadmills go nowhere. If you find yourself on a tapeout treadmill, get off. It is likely an indicator that your innovation is mismanaged and heading nowhere.

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ES3: How to Achieve 1000× More Wireless Data Capacity? 5G?



Organizer/Chair: **Eric Klumperink,** *University of Twente, Enschede, The Netherlands*

Co-organizers: **Sven Mattisson,** *Ericsson, Lund, Sweden*
Vojkan Vidojkovic, *Intel, Duisburg, Germany*

Exponential growth cannot go on forever, but wireless data growth still does. Especially video and Cloud services drive wireless data consumption, and 1000x in data capacity is targeted in the next 10 years. 5G is in the process of being defined and may include data rates at Gb/s, seamless integration of wireless LAN, short latencies, expansion into mm-Wave, and massive MIMO. The envisioned systems likely reach the limits of Shannon's capacity and will exploit additional degrees of freedom. A group of experts has been invited to share their thoughts on key new technologies and their path to implementation.

Speakers and Subjects

Challenges and Ideas for Wireless Networks
Tod Sizer, *Bell Laboratories/Alcatel-Lucent, New Providence, NJ*
This talk will discuss the key technology trends that will define the future of wireless networking, focusing on the key role of the network in a world increasingly defined by connecting tablets and machines to the Cloud. The need for a new paradigm of user-centric networking – what could be described as 'The Network of You', where the network becomes in essence a 'digital skin' – will be discussed as well as the associated new wireless network architecture required. This new architecture will be highly distributed, cell-less, and multi-radio access and will take advantage of any spectral resources, reusing these resources in a way that is continuously optimized per-user, per-application, per-location and per-network state. The impact these trends will have on the constituent wireless component technologies will also be highlighted.

Shannon's Capacity Meets Moore's law - The 5G Terminal Perspective
Asha Keddy, *Intel, Beaverton, OR*
While 1G-3G standards were focused on improving communications, and 4G was about data, we expect that the next-generation aka 5G will need to solve a more complex challenge: *how to enable communications + computing together*. Processing power, intelligence and communication capabilities will likely no longer exist just "here" and "there," but will be diffused across networks and mobile devices, enabling even the smallest of connected devices to do heavy computational tasks and support rich content and services. Perceptual computing and proximity communication will merge, and local sensing, communication, content distribution and processing will become essential. Significant extra capacity and ultra-low latency will enable operators to deliver a better user experience and to expand their value-added applications to new vertical markets such as healthcare, education, automotive and others. This talk explores these trends from a terminal perspective including Moore's law, Shannon's law and the role of new IC technologies to make this happen.

More Bits via the Same Spectrum - Massive MIMO Opportunities
Fredrik Tufvesson, *Lund University, Lund, Sweden*
Massive MIMO is one of the strong candidates to be included in next generation wireless systems and 5G. The technology offers the possibility to increase the spectral efficiency as well as the energy efficiency significantly compared to the solutions today, and we aim for an improvement by a factor of ten in both. In this talk we will describe the opportunities and challenges of Massive MIMO from a hardware perspective, with special emphasis on the experience we have obtained from the Lund University Massive MIMO test bed, LuMaMi. This test bed comprises 100 parallel coherent RF chains, feeding as many antenna elements, and can handle real-time video streaming to up to ten simultaneous users in a dynamic environment.

5G Radio Access – Requirements, Concept, and Technical Challenges
Yoshihisa Kishiyama, *NTT DOCOMO, Yokosuka, Japan*
5G will need to meet very challenging requirements and cover a wide range of scenarios and services. The evolution path and the system concept of 5G radio access are quite important for successful migration from LTE-Advanced (4G) to 5G and effective integration of key radio-access technologies. In this talk, we present our evolution concept and key radio-access technologies towards 5G. Efficient integration of lower and higher frequency bands is emphasized, to meet the challenges of achieving a 1000-fold increase in the system capacity and a 100-fold increase in the typical data-rate for wide coverage areas of cellular networks. Moreover, our recent activities and experimental trials for 5G radio access will be discussed.

SC1: *Circuit Design in Advanced CMOS Technologies: How to Design with Lower Supply Voltages*

Wim Dehaene, *KU Leuven, Leuven, Belgium*

Technology scaling brings lower supply voltages. For advanced CMOS technology nodes of 40nm and beyond, this leads to specific challenges. In particular, analog circuits require specialized design approaches and innovative techniques. Maintaining high precision with reduced available signal swing while keeping energy consumption within reasonable bounds has presented challenges for many circuit designers. Increased technological variability and leakage only make this worse.

This short course provides an overview of the challenges and solutions of modern circuit design in advanced technologies with low supply voltage. The course will start with a system overview of the problem. Then, several types of circuits will be discussed. General analog and mixed-mode building blocks, A/D converters and RF components each are the subject of a separate talk.

OUTLINE

A Roadmap to Lower Supply Voltages – A System Perspective

Jan Rabaey, *University of California, Berkeley, CA*

A novel class of devices that broadly fall under the rubrics of "Internet-of-things" and "wearable" may soon upend the unprecedented growth in mobile devices that we have witnessed over the past decades. For these devices to be viable, however, a continuous reduction in energy-per-operation is necessary. Unfortunately, the flattening of traditional semiconductor scaling means that only a small part of this reduction can be expected from technology advances. The good news is that one design parameter that has a huge impact on energy consumption - the supply voltage - is still substantially above the fundamental limits (at least for digital circuits). Hence this leaves ample room for innovative design techniques to explore further lowering of the supply voltage.

The largest hindrances to low supply voltages are leakage and uncertainty. The presence of leakage sets a minimum voltage (and energy) for digital operation in a given technology. Going beyond that requires an aggressive energy-management strategy. Addressing uncertainty (arising from process variations, temporal changes and data statistics) typically requires margins to ensure functionality and correctness. Hence techniques to minimize margining while guaranteeing correct operation are important. Both leakage and uncertainty management can be performed at many layers of the design hierarchy. In this lecture, we will present an overview of commonly used and emerging techniques, illustrated with industrial and academic examples.

About the presenter:
Jan Rabaey received his Ph.D. degree in applied sciences from the Katholieke Universiteit Leuven, Belgium. In 1987, he joined the faculty of the Electrical Engineering and Computer Science department of the University of California, Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship. He is currently the scientific co-director of the Berkeley Wireless Research Center (BWRC), as well as the founding director of the Berkeley Ubiquitous SwarmLab.

Prof. Rabaey has made widely recognized contributions to a number of domains, including advanced wireless systems, sensor networks, configurable circuits and low-power design. His current interests include the conception and implementation of next-generation integrated wireless systems over a very broad range of applications, as well as exploring the interaction between the cyber and the biological world.

He is the recipient of a wide range of major awards, including the Semiconductor Industry Association (SIA) University Researcher Award. He is an IEEE Fellow and a member of the Royal Flemish Academy of Sciences and Arts of Belgium, and has been involved in a broad variety of start-up ventures.

Designing Ultra-Low-Voltage Analog and Mixed-Signal Circuits

Peter Kinget, *Columbia University, New York, NY*

This talk focuses on the challenges and solutions for designing analog circuits at supply voltages well below 1V. Fundamental limitations of the MOS transistor force us to rethink the most basic analog circuit configurations. At the same time, low-voltage operation offers new opportunities to use all four terminals of the transistor while the speed of nanoscale devices allows for different representations for analog signal information. The lecture discusses solutions for analog building blocks like amplifiers operating at ultra-low supply voltages, and how they can be used to build complete analog signal processing systems like filters, track-and-hold circuits or analog-to-digital converters.

About the presenter:
Peter R. Kinget received an engineering degree in electrical and mechanical engineering and the Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium. He has worked in industrial research and development at Bell Laboratories, Broadcom, Celight and Multilink before joining the faculty of the Department of Electrical Engineering, Columbia University, NY in 2002, where he is currently a Professor. He is also a consulting expert on patent litigation and a technical consultant to industry. His research interests are in analog, RF and power integrated circuits and the applications they enable in communications, sensing, and power management.

Dr. Kinget is a Fellow of the IEEE and is widely published. He is a co-recipient of several awards including the "First Prize" in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge and the "2011 IEEE Communications Society Award for Advances in Communication." He has been a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society (SSCS), and an Associate Editor of the IEEE Journal of Solid State Circuits and the IEEE Transactions on Circuits and Systems II. He has served on the program committees of many of the major solid-state circuits conferences and currently is an elected member of the IEEE SSCS Adcom.

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ADC Design in Scaled Technologies

Andrea Baschirotto, *University of Milan-Bicocca, Milan, Italy*

This talk focuses on recent developments in ADCs, which are one of the primary components in any mixed-signal integrated system.

The first part reviews the most relevant changes in MOS transistor behaviour when realized in scaled technologies (VDD reduction, gain reduction, VTH deviation, higher speed, etc.), focusing on how they affect ADC design.

After this, general trends in ADCs in the recent literature are analyzed, and the reported ADC implementations in the 32nm or below technologies are presented, looking at their innovative solutions, emphasizing the common trends and the difference between the several implementations.

About the presenter:
Andrea Baschirotto received his Ph.D. in electronics engineering in 1994 from Univ. Pavia. He is an Associate Professor at Univ. Milan-Bicocca, Italy. His main research interests are in the design of CMOS mixed analog/digital integrated circuits, in particular for low-power and/or high-speed signal processing. He participated in several research collaborations (also funded by National and European projects) and several collaboration between Universities and Industries. In 2010 he co-founded the start-up sparklingIC, of which he serves as CTO.

He has authored or co-authored more than 190 papers in international journals and presentations at international conferences, 6 book chapters, and holds 35 US patents. In addition, he has co-authored more than 120 papers within research collaborations on high-energy physics experiments.

Andrea Baschirotto has been Associate Editor of several IEEE journals. He has been the Technical Program Committee Chairman for ESSCIRC 2002. He is or was member of the Technical Program Committee of several international conferences (ISSCC, ESSCIRC, AACD, DATE, etc.). Since 2005, he is serving the ESSCIRC TPC as Data Converter Subcommittee Chairman. He has been the secretary of the European Committee of ISSCC Technical Program Committee. He is an IEEE Fellow (2013). He is the founder (2006) and the Chairman of the IEEE Solid-State Circuit Society Italian Chapter.

Ultra-Low-Voltage RF Circuits and Transceivers

Hyunchol Shin, *Kwangwoon University, Seoul, Korea*

The continuing scaling of CMOS technology and the growing needs for single-cell battery operation drive the supply voltage of RF circuits toward the sub-1V region. As the supply voltage approaches only 2-3 times Vth, many traditional RF circuit topologies are becoming ineffective. Much effort has been spent rethinking the conventional circuit topologies and radio architectures for RF applications. This presentation focuses on the design issues and recent progress in transceiver architectures and building blocks to meet the sub-1V challenge.

The first part reviews several sub-1V design techniques that can be applied to many RF circuits. The second part covers the receiver and its key building blocks (LNA and mixer) discussing design fundamentals, advanced circuit topologies, and recent implementation examples for sub-1V operation. The third part covers the most power-hungry parts in RF transceivers, namely the VCO, frequency divider, and PLL synthesizer. The presentation concludes by explaining the opportunities that are yet to come.

About the presenter:
Hyunchol Shin received the Ph.D. degree in electrical engineering from KAIST, Korea in 1998. After his Ph.D., he had gained professional experience at several institutions and companies, such as Samsung Electronics, Korea, University of California, Los Angeles, CA, Qualcomm, San Diego, CA, all working on RF/analog circuit design for wireless communications. Since 2003, he has been with Kwangwoon University, Seoul, Korea, where he is currently a Professor. From 2010 to 2011, he took a sabbatical leave at Qualcomm Corporate R&D, San Diego, CA. His research focuses on CMOS RF/analog/microwave circuits and PLL frequency synthesizers.

Prof. Shin has (co)authored over 70 journal and conference papers and holds 30 patents in the field of RF/analog circuit design. He is a senior member of the IEEE, and has served on the technical program committees of several IEEE conferences such as ISSCC, A-SSCC, MWSCAS, RFIT, ISOCC, and IWS.

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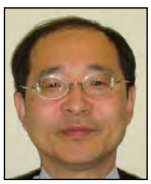

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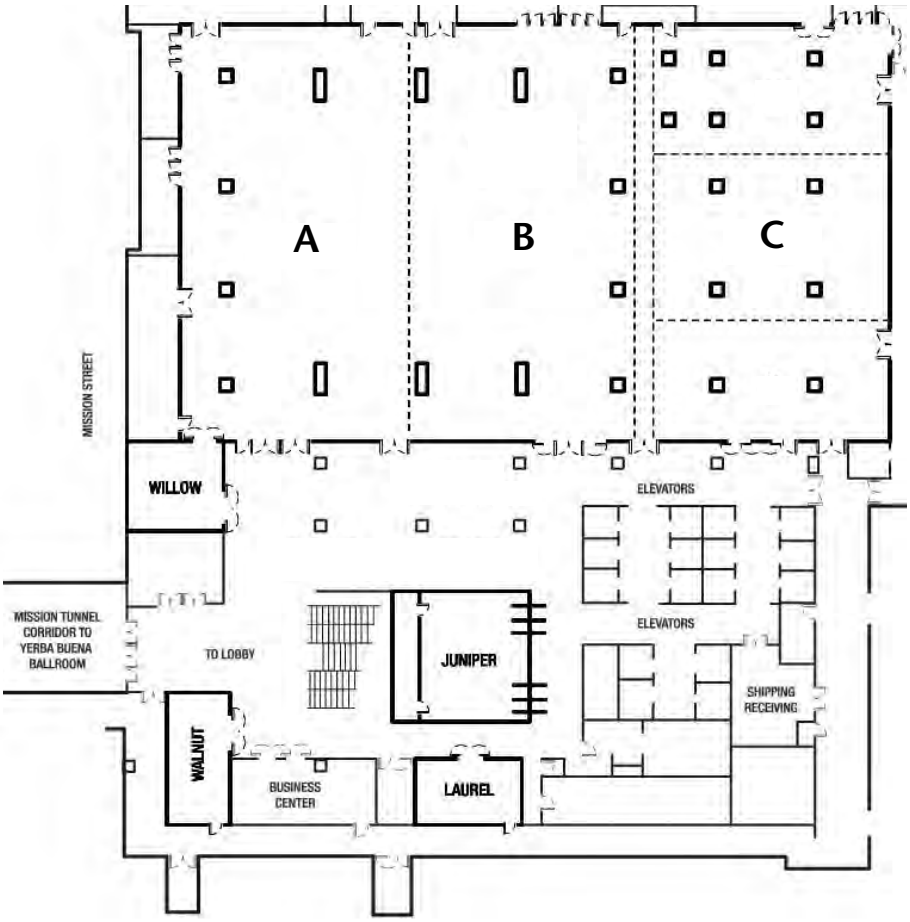

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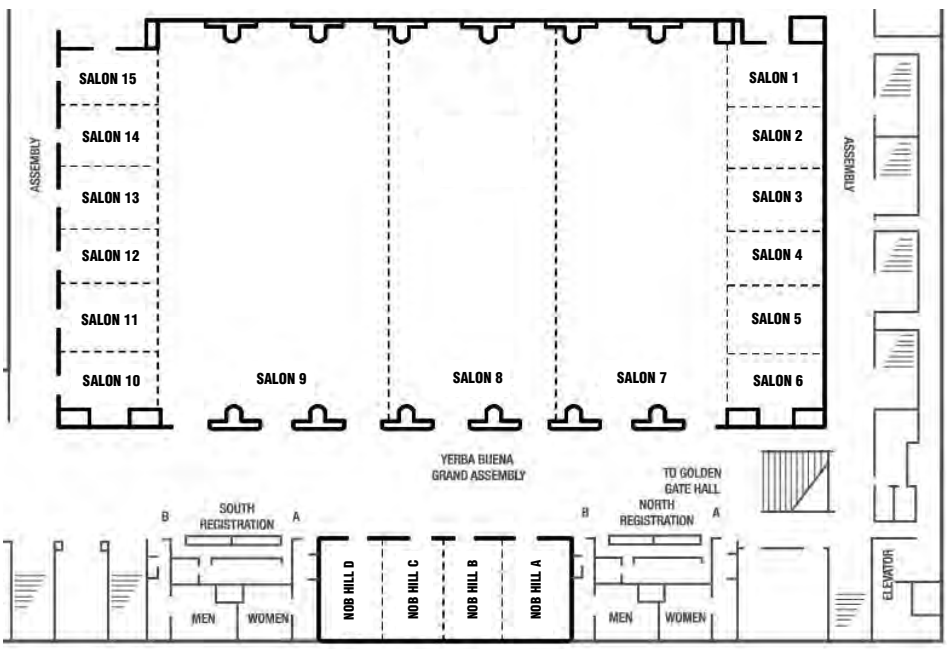

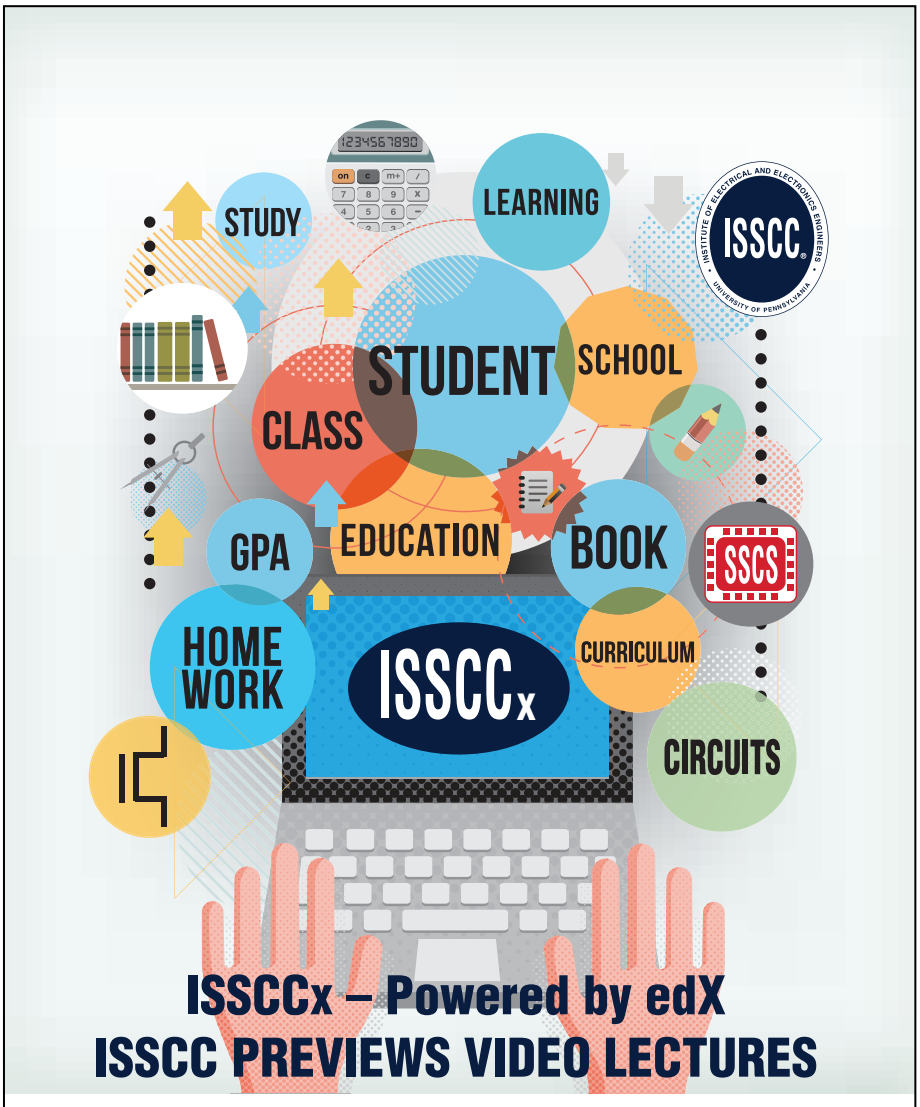

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Innovative and original papers are solicited in subject areas including (but not limited to) the following:

ANALOG — Op-amps and instrumentation amplifiers, comparators, power control and management circuits, voltage references, regulators, DC-DC converters, energy-scavenging circuits; filters, continuous-time and discrete-time; nonlinear analog circuits, switched-capacitor circuits; oscillators, synthesizers, PLLs; very-low-power and low-voltage analog circuits, digitally-assisted analog circuits.

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WIRELESS — Wireless systems (receivers, transmitters, transceivers, SoCs, SiPs) with focus on standards-based applications up to 100GHz; applications in cellular, WLAN, BT, GPS, BAN, GPS, TV tuner, UWB, ISM, WiMax, WiGig, broadcast, radar, imaging, low-power, multi-standard and multi-band; innovative system architectures and solutions for advanced wireless applications.

WIRELINE — Receivers/transmitters/transceivers for wireline systems, including backplane transceivers, optical links, chip-to-chip communications and 3D structures; applications in designs for (but not limited to) Ethernet, Fibre Channel, optical/electrical data transfer, PON, advanced serial memory, consumer product wired communication, SONET, SDH, FDDI, and xDSL; wireline transceiver building blocks such as AGC, equalization circuits, oscillators, PLLs, line drivers, and hybrids.

Submission Deadline is Monday, September 14, 2015 • 3:00PM Eastern Daylight Time (19:00 GMT)

STUDENT INITIATIVES

Graduate students are invited to participate in opportunities to showcase ongoing work and exchange experiences with other students and researchers from academia and industry. These include the Student Research Preview and the Silkroad Award (to a first-time student presenting author of a regular paper from an emerging region in the Far East).

Further information including submission procedures, formats, student initiatives and deadlines can be found at http://www.isscc.org

Sunday, February 22nd	ISSCC 2015 TUTORIALS		
8:30AM	**T1:** Fundamentals of Modern RF Receivers	**T2:** Basics of DRAM Interfaces	**T3:** Ultra-Low-Power Wireless Systems
10:30AM	**T4:** Low-Power Near-Threshold Design	**T5:** High-Speed Current-Steering DACs	**T6:** Clock and Data Recovery Architectures and Circuits
1:30PM	**T7:** Basics of Many-Core Processors	**T8:** Analog Techniques for Nano-Power Circuits	
3:30PM	**T9:** Frequency Synthesizers for Wireless Transceivers	**T10:** CMOS Sensors for 3D Imaging	
	ISSCC 2015 FORUMS		
8:00AM	**F1:** High-Speed Interleaved ADCs	**F2:** Memory Trends: From Big Data to Wearable Devices	

Events below in Bold Box included in Conference registration

	ISSCC 2015 EVENING SESSIONS				
	7:30 PM ES1: Student Research Peview: Short Presentations with Poster Session		**8:00 PM ES2:** Brain-Machine Interfaces: ICs Talking to Neurons		
Monday, February 23rd	ISSCC 2015 PAPER SESSIONS				
8:30AM	**Session 1:** Plenary Session				
1:30PM	**Session 2:** RF TX/RX Design Techniques	**Session 3:** Ultra-High-Speed Wireline Transceivers and Energy-Efficient Links	**Session 4:** Processors	**Session 5:** Analog Techniques	**Session 6:** Image Sensors & Displays
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour				
	ISSCC 2015 EVENING SESSIONS				
8:00PM	**EP1:** Moore's Law Challenges Below 10nm: Technology, Design, & Economic Implications		**EP2:** Lost Art? Analog Tricks and Techniques from the Masters		
Tuesday, February 24th	ISSCC 2015 PAPER SESSIONS				
8:30AM	**Session 7:** Non-Volatile Memory Solutions	**Session 8:** Low-Power Digital Techniques	**Session 9:** High-Performance Wireless	**Session 10:** Advanced Wireline Techniques & PLLs	**Session 11:** Sensors & Imagers for Life Sciences
1:30PM	**Session 12:** Inductor-Based Power Conversion	**Session 13:** Energy-Efficient RF Systems	**Session 14:** Digital PLLs & SoC Building Blocks	**Session 15:** Data-Converter Techniques	**Session 16:** Emerging Technologies Enabling Next-Generation Systems
5:15PM	Demonstration Session (4:00-7:00 PM), Author Interviews, Social Hour				
	ISSCC 2015 EVENING SESSIONS				
8:00PM	**EP3:** Innovating on the Tapeout Treadmill		**ES3:** How to Achieve 1000x More Wireless-Data Capacity. 5G?		
Wednesday, February 25th	ISSCC 2015 PAPER SESSIONS				
8:30AM	**Session 17:** Embedded Memory & DRAM I/O	**Session 18:** SoCs for Mobile, Vision, Sensing, & Communications	**Session 19:** Advanced Wireless Techniques	**Session 20:** Energy Harvesting & SC Power Conversion	**Session 21:** Innovative Personalized Biomedical Systems
1:30PM	**Session 22:** High Speed Optical Links	**Session 23:** Low-Power SoCs **Session 24:** Secure, Efficient Circuits for the Internet of Things (IoT)	**Session 25:** RF Frequency Generation from GHz to THz	**Session 26:** Nyquist-Rate Converters	**Session 27:** Physical Sensors
5:15 PM	Author Interviews				

Thursday, February 26th	ISSCC 2015 SHORT COURSE			
8:00 AM	**SC1:** Circuit Design in Advanced CMOS Technologies: How to Design with Lower Supply Voltages			
	ISSCC 2015 FORUMS			
8:00AM	**F3:** Cutting The Last Wire – Advances in Wireless Power	**F4:** Building the Internet of Everything (IoE): Low-Power Techniques at the Circuit & System Levels	**F5:** Advanced RF CMOS Transmitter Techniques	**F6:** IO Design at 25Gb/s and Beyond

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