27.8 A 4600μm² 1.5°C (3σ) 0.9kS/s Thermal-Diffusivity Temperature Sensor with VCO-Based Readout

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Temperature sensors are widely used in microprocessors to monitor on-chip temperature gradients and hot-spots, which are known to negatively impact reliability [1-4]. Such sensors should be: 1) Small to facilitate floor planning; 2) Fast to track millisecond thermal transients and 3) Easy to trim to reduce the associated costs. Recently, it has been shown that thermal diffusivity (TD) sensors can meet these requirements [5]. TD sensors operate by digitizing the temperature-dependent delay associated with the diffusion of heat pulses through an electro-thermal filter (ETF), which, in standard CMOS, can be readily implemented as a resistive heater surrounded by a thermopile. Unlike BJT-based temperature sensors, their accuracy actually improves with CMOS scaling [6], since it is mainly limited by the accuracy of the heater/thermopile spacing, which in turn is determined by lithography. However, the readout circuitry of prior TD sensors has been based on analog phase-domain ΔΣ ADCs, which are not easily ported to low-voltage technologies, and which occupy much more area than the ETF itself [5].

This paper presents a highly digital TD sensor in 0.16μm CMOS with ±1.5°C (3σ, single trim) inaccuracy and achieving 0.6°C resolution at a 0.9kS/s sampling rate. The sensor occupies only 4600μm², which is 40% less than [5], and which compares favourably to state-of-the-art sensors with similar accuracy and sampling rates [1-4]. This advance is mainly enabled by the adoption of a highly digital VCO-based phase-domain ΔΣ ADC.

Figure 27.8.1 shows the block diagram of the proposed TD sensor. It consists of an ETF, a gm stage, a current-controlled oscillator (CCO) and a 6b up/down counter. The gm stage and the CCO realize a VCO, which converts variations in the ETF's output voltage into variations in the CCO's frequency. After conversion to the frequency domain, the phase shift of the ETF (ΦETF) is then digitized by a 1st-order phase-domain ΔΣ modulator. Unlike the amplitude-domain modulator used in [5], which was based on a chopper demodulator and a gm-C integrator, the modulator used here is based on a simple up-down counter. Since the input is now in the frequency domain, the counter replaces the integrator, while its up-down input, Fchop, emulates the action of the chopper demodulator, i.e. determining whether the counter's state is either incremented or decremented. The counter's output is sampled and quantized by latching its most significant bit (MSB). The resulting output bitstream (BS) then switches Fchop between FΦ0 and FΦ1 in a ΔΣ manner. Thanks to the compact footprint of the CCO and the counter, the area of the proposed read-out circuit is much smaller than that of the capacitor-dominated gm-C-based solution. The requirements on the gm stage are also relaxed, since its gain no longer affects sensor accuracy. Moreover, the offset currents introduced by the high-frequency switching action of an analog chopper are eliminated, thus obviating the need for the system-level chopping used in [5].

An external 75MHz clock (Fsync) is used to generate a 1.17MHz ETF drive signal (Fdrive) and two reference 1.17MHz clocks (FΦ0 and FΦ1) with phase shifts Φ0 and Φ1, respectively. Each of these phase-shifts can be independently adjusted in 5.625° steps spanning a phase range from 0 to 90°. As in [5], an incremental two-step (zoom) conversion is adopted. During the coarse conversion, Φ0 and Φ1 are set to 0 and 90° to cover the full temperature range, and a 128-step conversion is used to obtain a 4b estimate of the ETF's phase, Φcoarse. Φ0 and Φ1 are then set to straddle Φcoarse, such that Φ1-Φ0 = 33.75°. A 1024-step fine conversion is then initiated to accurately determine the ETF's phase shift, Φfine. A full zoom ADC conversion requires 1272 clock samples (including 110 samples for CCO frequency trim) at a sampling rate of 1.17MHz, resulting in a conversion rate of 0.9kS/s.

Figure 27.8.2 shows the timing diagram of the ΔΣ loop, for the situation when the CCO's frequency, Fcco, is modulated by the ETF's output voltage at Fdrive. The value accumulated by the counter after one complete up/down cycle will then be proportional to the integrated phase-shift between the modulated frequency and the up/down control signal Fchop. For instance, if the two signals are exactly in phase, the counter state will increment (or decrement) steadily, while if their phase-shift is 90°, the counter state will remain unchanged, as it will be incremented and decremented in exactly the same way during both states of Fchop. Since the duty-cycle of Fchop is exactly 50%, the frequency of the CCO is not critical. However, it should be much higher than Fdrive to minimize quantization errors in the digitized phase shift accumulated by the counter.

The circuit diagram of the gm stage and the CCO is shown in Fig. 27.8.3. Unlike [5], the relaxed gain requirements mean that the gm stage can be realized by a simple differential pair with a current mirror load. However, the phase shift and spread of the RC filter formed by its input capacitance and the resistance of the thermopile will be indistinguishable from the ETF's phase shift. To minimize this, the input devices of the single-stage OTA are near-minimum size and are cascoded for maximum bandwidth. The CCO is a minimum-size 3-stage ring oscillator, which has been optimized for highest current-to-frequency gain. In order to fix the operating point of the CCO, a 6b current DAC (IDAC) is used to trim the offset of the gm-stage and the spread of the CCO before every conversion. During the trimming phase, the MSB-1 bit of the counter is compared to a reference clock. Depending on the result, the IDAC value is updated by a ramp-search algorithm to fix the CCO output frequency to 220MHz. Although the counter output is insensitive to variations in the nominal CCO frequency, trimming is necessary to avoid exceeding the maximum operating frequency of the counter when Fcco is too high, or introducing too much quantization noise when Fcco is too low.

An array of 5 TD sensors (highlighted in the die photo, Fig. 27.8.7) has been realized in a standard 0.16μm 1P5M CMOS process. The total power consumption of each sensor is 3.6mW, with 50% and 40% of the power dissipated in the ETF's heater and the counter, respectively. In order to demonstrate the low-voltage capability of the proposed architecture, the supply of the analog section (gm stage, CCO and IDAC) was set to 1.35V for all reported measurements, while the digital supply was kept at the standard 1.8V so as not to limit counter speed. Fig. 27.8.4 shows the FFT of the output bitstream during a fine conversion. The thermal noise floor corresponds to a resolution of 0.6°C (rms) in a 1.1ms conversion time. As shown in Fig. 27.8.5, the estimated inaccuracy of 80 sensors (16 samples) after a single point temperature trim at 65°C, as is typical in microprocessor applications [1], is ±1.5°C (3σ) from -10 to 125°C.

The performance of the sensor is summarized in Fig. 27.8.6 and compared to that of other sensors intended for microprocessor monitoring. Due to the additional delay and noise introduced by the CCO, the sensor's accuracy and resolution are somewhat degraded with respect to prior TD sensors employing a more analog read-out [5]. However, after a one-point-trim, it is still more accurate than other state-of-the-art BJT- or delay-based temperature sensors intended for thermal monitoring applications. It is also the second smallest, which demonstrates the advantages of the proposed highly digital read-out architecture, despite its realization in a mature 0.16μm CMOS process. Since 70% of the sensor's area is occupied by digital circuitry, porting the sensor to a 32nm process should reduce the digital area by 20×, and thus reduce the total sensor area to less than 1650μm².

Acknowledgements:
The authors thank Mike Perrott for introducing us to the joys of CppSim.

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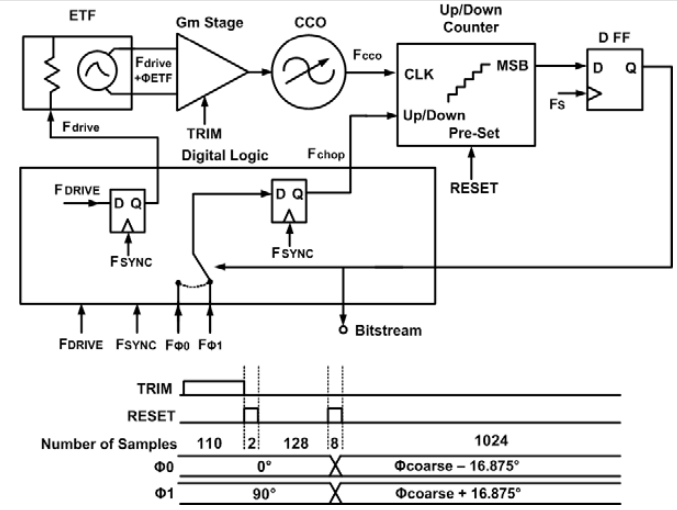

Figure 27.8.1: Block diagram of the proposed thermal diffusivity temperature sensor with a VCO-based phase domain ΔΣ modulator, and the accompanying timing diagram.

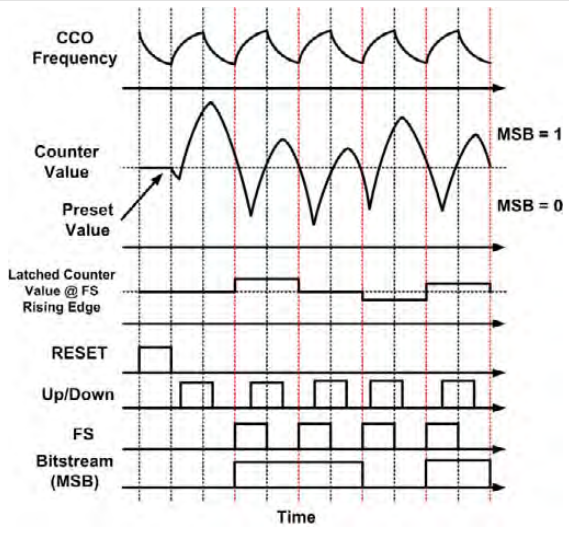

Figure 27.8.2: Timing diagram showing the ΔΣ action of the VCO and the up/down counter combination.

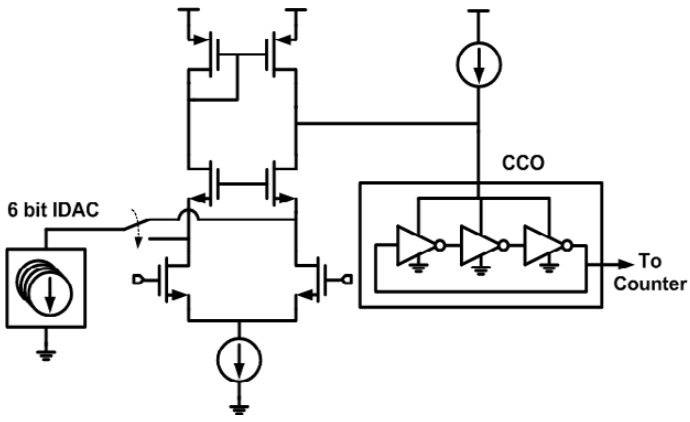

Figure 27.8.3: Circuit schematic of the analog front-end (gm stage and CCO) of the proposed temperature sensor.

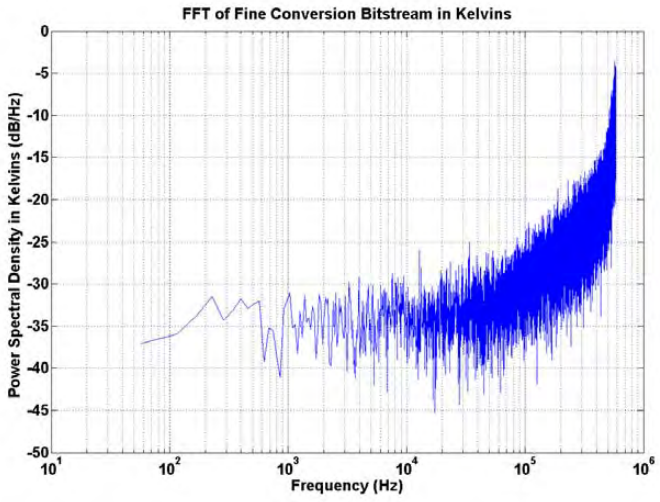

Figure 27.8.4: FFT of the phase-domain ΔΣ modulator bitstream during fine conversion with 122880 samples, rectangular window, averaged over 6 FFTs.

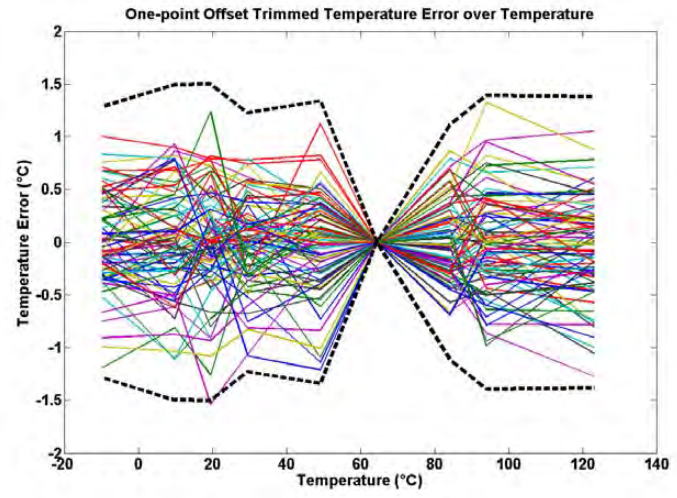

Figure 27.8.5: Measured sensor-to-sensor temperature errors for 16 chips (80 sensors) after single-point trimming at 65°C. Bold dotted lines indicate 3σ limits.

	This Work	[1]	[1]	[2]	[3]	[4]	[5]
Technology	160nm	32nm	22nm	32nm	65nm	32nm	160nm
Sensor Type	TD	BJT	BJT	BJT	Delay	Diode	TD
Inaccuracy (3σ) Untrimmed	±6.5°C	-	-	±5°C	-	-	±2.4°C
Single Temp. Trim	±1.5°C	±4.5°C	-	-	±1.5°C *	-	±0.65°C
Two Temp. Trim	-	±1.2°C	±1.5°C	-	-	±1.95°C	-
Temp. Range	-10 - 125 °C	20 - 110 °C	-10 - 110 °C	-10 - 110 °C	0 - 110 °C	0 - 100 °C	-40 - 125 °C
Area (mm²)	0.0046	0.02	0.006	0.02	0.008	0.001	0.008
Resolution (RMS)	0.6°C	0.19°C	0.25°C	0.15°C	0.94°C	0.25°C	0.2°C
Speed	0.9kS/s	2kS/s	1.4 kS/s	1.2kS/s	469kS/s	2.5kS/s	1kS/s
Power	3.6mW	3.78mW	1.35mW	1.6mW	0.5mW	0.5mW	3.1mW

* Peak to peak error variation

Figure 27.8.6: Performance summary and comparison with previous work.

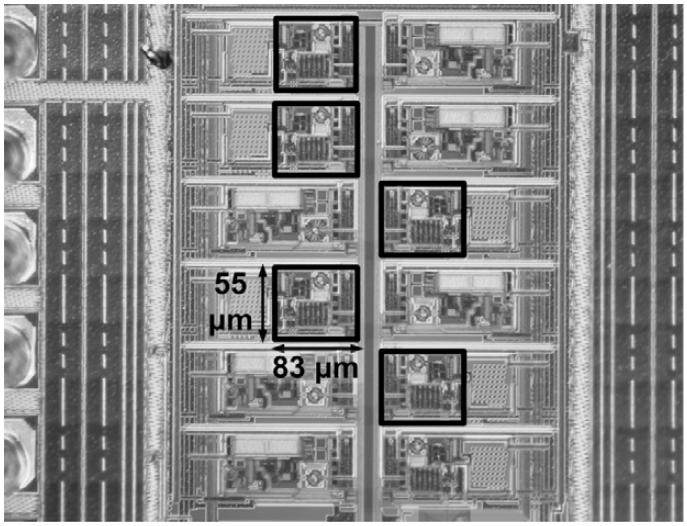

Figure 27.8.7: Die micrograph with individual temperature sensors highlighted.

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