27.7 A 0.05mm² 1V Capacitance-to-Digital Converter Based on Period Modulation

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This paper presents a digitally assisted period modulation (PM)-based capacitance-to-digital converter (CDC) that is >9× smaller than prior CDCs with >10b resolution [1-4], and improves the energy efficiency by >10× compared to previous PM-based CDCs [1]. This is achieved with the help of a piece-wise charge transfer technique that eliminates the need for a large on-chip integration capacitor, a dual-integration-capacitor scheme that reduces the front-end noise contribution, a sampled-biasing technique that reduces the noise of the integration current, and a current-efficient inverter-based design.

The CDC is based on a relaxation oscillator whose output period is proportional to the sensor capacitance, C (Fig. 27.7.1) [1]. It employs an active integrator, on which charge proportional to C is balanced over time against charge provided by a pair of current sources, I_{int}. After an initial reset, which clears the integration capacitor, C_{int}, a first phase ϕ_1 starts. The drive side V_{drive} of C is pulled to V_{DD}, causing a charge $V_{DD}C$ to be transferred to C_{int}. This charge is then removed by a sinking current, I_{int}, until the integrator output, V_{int}, returns to its initial value. This is detected by a comparator, whose output transition initiates the next phase, ϕ_2, during which the drive side is pulled to ground. The associated charge transfer is compensated similarly by a sourcing current, I_{int}, initiating upon completion a new phase ϕ_1. This process repeats N times, leading to a total time period of $T = NV_{DD}C / I_{int}$. By counting the number of cycles of a reference clock during this period, a digital representation of C is obtained.

Since T_x depends on the absolute values of V_{DD} and I_{int}, its sensitivity to C is not well defined. Moreover, circuit non-idealities such as comparator delay give rise to offset errors. To nevertheless obtain a well-defined capacitance-to-digital conversion, an auto-calibration scheme is applied to obtain a full scale defined by a reference capacitor, C_{ref} [1]. In three subsequent measurements, an offset capacitor C_0, $C_x + C_0$, and $C_{ref} + C_0$ are connected (Fig. 27.7.1). This leads to three time periods T_0, T_x, and T_{ref}, which are, as before, quantized using a counter, and used to calculate, in digital post-processing, a final ratiometric output $M = (T_x - T_0) / (T_{ref} - T_0) = C_x / C_{ref}$. Any offset and gain errors in the time periods cancel in this ratio [1]. This allows the integrator and the comparator to be implemented using simple inverters as amplifiers.

An important limitation of the circuit of Fig. 27.7.1 is that the noise of the integrator and that of the comparator cause an accumulating jitter on the measurement time T (i.e. either T_0, T_{ref}, T_x). Suppose, for instance, that noise causes the detection of the zero crossing at the end of ϕ_1 to happen late (see Fig. 27.7.3). This timing error is not repaired later and thus causes jitter on T, as do similar errors on the other zero crossings. Prior implementations of period-modulator-based CDCs [1] suffer from similar jitter-accumulation problems.

Here, this problem is solved by employing two integration capacitors, C_{int1} and C_{int2}, one for each phase (Fig. 27.7.2). Consider a similar noise-induced timing error as before. The error charge associated with this error is now kept on C_{int1}, and causes the next phase ϕ_1 to be shorter, exactly compensating for the timing error. Noise-induced timing errors on all transitions are thus cancelled, except for those on the last phases of T. Thus, the overall impact of integrator and comparator noise is strongly reduced.

The integration current sources have been implemented using resistively degenerated MOS current sources. To prevent the bias circuit of these sources from adding noise, a sample-and-hold (S/H) circuit is added at their gates. This samples the noise at the gate and holds it constant during the measurement, allowing it to be compensated by the auto-calibration scheme, which also suppresses the low-frequency noise of the current sources themselves.

An additional limitation of the circuit of Fig. 27.7.1 is that it requires an integration capacitor that is at least as large as the sensor capacitor, to prevent the output of the integrator from clipping. In applications where C_x is a relatively large external sensor capacitor, the resulting die-size penalty is highly undesirable. In [1], this problem is addressed by adding a continuous-time feedback loop from the integrator output to the drive side of the sensor so as to limit the rate at which V_{drive} changes when the integrator output becomes too large. This loop, however, is potentially unstable and consumes extra power.

Here, instead, we apply a simpler solution that involves driving the sensor using switched current sources instead of hard-switching it to the supplies (Fig. 2.7.2). These current sources still pull V_{drive} up and down between V_{DD} and ground, but can be temporarily switched off if V_{int} becomes too high (Fig. 27.7.3). Two comparators with hysteresis connected to V_{int} detect if this is the case and activate a signal $limit_H$ or $limit_L$ that interrupts the current. As a result, the charge transfer from C_x to C_{int} will be periodically interrupted, ensuring that V_{int} remains bounded even if C_{int} is much smaller than C_x (Fig. 27.7.3). The two extra comparators have been implemented using simple Schmitt-trigger logic gates in which the transistors have been sized to obtain appropriate threshold levels relative to the integrator output range. To ensure that, at the end of the phase, the full charge transfer is completed, an additional switch in parallel wtih the current sources hard-switches the drive side to the supplies just before the integrator output returns to zero (signals $hard_H$ and $hard_L$). Thus the initial and final conditions of the charge transfer are not affected by this scheme, ensuring that the accuracy of the charge transfer is maintained. The hard switching is activated by the main comparator, whose threshold is initially slightly shifted up or down by activating an additional PMOS or NMOS at the inverter output using control signals *thld_up* and *thld_dn*. After activation of the hard switching, the threshold returns to its original value, so that the comparator can detect, as before, the end of the phase.

The CDC is implemented in a 0.16µm CMOS technology, and occupies an active area of 0.05mm² (Fig. 27.7.7), which includes two C_{int} of 4pF each, and C_0 of 4 pF. The counter used to digitize the time periods has been implemented in an FPGA for flexibility. The chip can be operated in two modes, in which the OTA g_m is 294µA/V and 580µA/V, and power consumption is 14µA and 21µA, respectively, from a 1.0V supply.

Figure 27.7.4 shows the resolution of the CDC as a function of C_x and as a function of the number of periods N. This measurement was performed using discrete off-chip capacitors connected as C_x, and an off-chip reference capacitor of 6.8pF. Without activating the S/H circuits in the integration current sources, the resolution is degraded due to the noise of the bias circuit. With the S/H enabled, a significant improvement is obtained. The results shown are for the low-g_m mode; the high-g_m mode provides comparable results. As shown, the CDC is capable of handling a wide range of capacitance values, far exceeding the reference capacitance and on-chip capacitance, making it very suitable for interfacing with larger off-chip sensor capacitors.

Figure 27.7.5 shows the result of a displacement measurement performed by connecting the CDC to a parallel-plate capacitor mounted on a linear displacement stage. To measure the non-linearity of the CDC, its readings were compared with those of a precision capacitance bridge (Andeen-Hagerling AH 2700A). In the low-g_m mode, the peak non-linearity is below ±2fF, while for the high-g_m mode it improves to less than ±0.25fF, which corresponds to 14b on the range of 8pF. Figure 27.7.5 also shows the result of a pressure measurement performed by connecting a MEMS pressure sensor to the CDC. Figure 27.7.6 summarizes the performance of the CDC and compares it to prior CDCs with >10b ENOB. Compared to prior CDCs based on period modulation [1], its energy consumption and die size are more than an order-of-magnitude smaller. Compared to other designs with comparable resolution [2-4], it is >9× smaller, making it an attractive candidate for area- and energy-constrained applications.

References:

[1] Z. Tan, et al., "An Energy-Efficient 15-Bit Capacitive-Sensor Interface Based on Period Modulation," *IEEE J. Solid-State Circuits,* vol. 47, no. 7, pp. 1703-1711, July 2012.

[2] X. Sha, et al., "A Capacitance-to-Digital Converter for Displacement Sensing with 17b Resolution and 20µs Conversion Time," *ISSCC Dig. Tech. Papers*, pp. 198-199, Feb. 2012.

[3] H. Ha, et al., "A 160nW 69.3fJ/conversion-step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes," *ISSCC Dig. Tech. Papers*, pp. 220-221, Feb. 2014.

[4] S. Oh, et al., "15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR," *IEEE Symp. VLSI Circuits*, June 2014.

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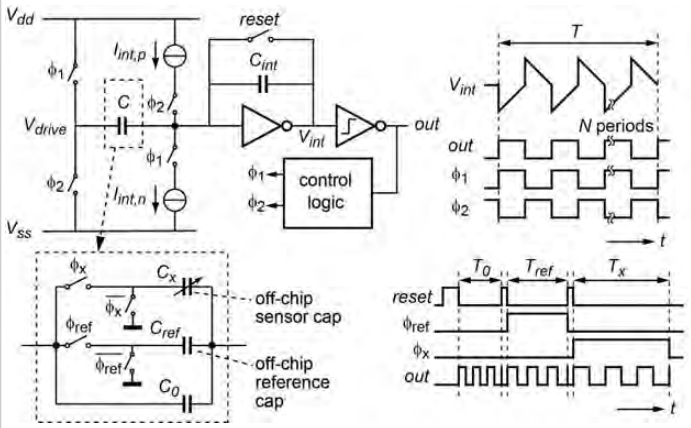

Figure 27.7.1: Operating principle of the capacitance-to-digital converter (CDC).

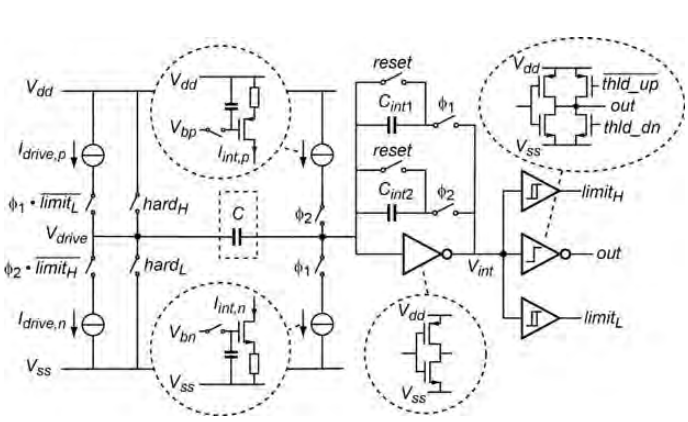

Figure 27.7.2: Circuit diagram of the period modulator.

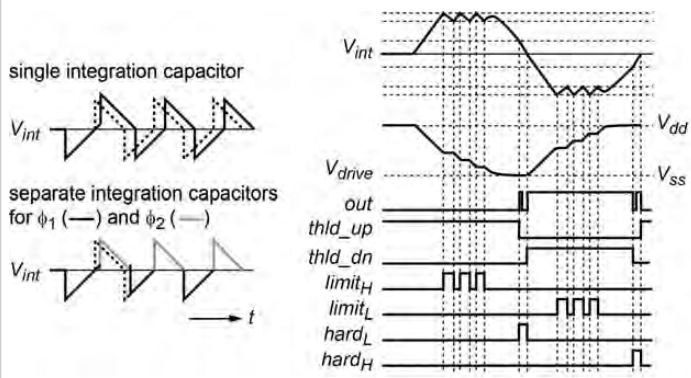

Figure 27.7.3: Timing diagrams illustrating the use of two integration capacitors and the piece-wise charge transfer mechanism that limits the integrator output swing.

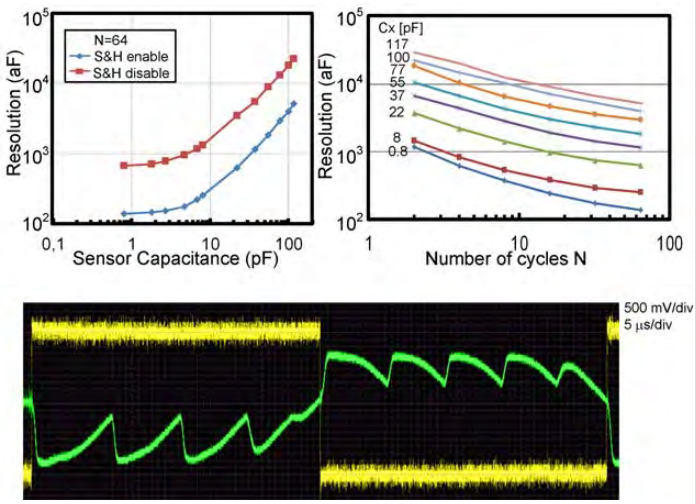

Figure 27.7.4: Measured resolution as a function of capacitance and number of cycles, and measured output voltage of the integrator showing the piece-wise charge transfer.

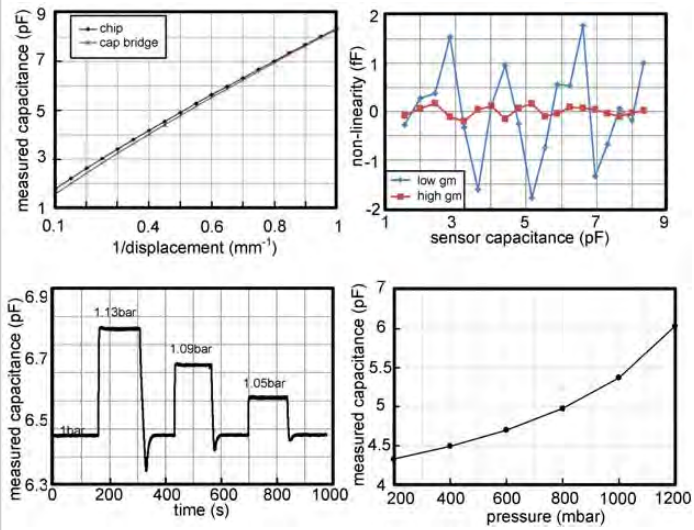

Figure 27.7.5: Measured capacitance as a function of displacement, with non-linearity, and measured capacitance as a function of pressure.

	[1]	[2]	[3]	[4]	This work	
Technology	0.35µm CMOS	0.35µm CMOS	0.18µm CMOS	0.18µm CMOS	0.16µm CMOS	
Type	PM	DS	SAR	DS + SAR	PM	
Supply voltage	3.3 V	3.3 V	1.2 V (Analog) 0.9 V (Digital)	1.4 V	1 V	
Supply current	64 µA	4.5 mA	N.A.	24 µA	14 µA	
Power	211 µW	14.9 mW	160 nW	33.7 µW	14 µW	
Input range (pF)	0 – 6.8	8.4 – 11.6	2.5 – 75.3	0 – 24	0 – 8 [1]	
Meas. time	7.6 ms	20 ms	4 ms	230 ms	0.21 ms (N=2)	6.86 ms (N=64)
Resolution (rms)	208 aF	65 aF	6 fF	156 aF	1443 aF	255 aF
ENOB (bit) [2]	13.5	13.80	11.8	15.44	10.6	13.1
FoM (pJ/step) [3]	138.6	20.9	0.181	0.175	1.87	10.6
Area (mm^2)	0.51	2.6	0.49	0.456	0.05	

[1] Chosen as example; the CDC can handle larger capacitances (see Fig. 4)

[2] $ENOB = \frac{SNR-1.76}{6.02}$, where $SNR = 20 \cdot \log(\frac{\frac{Full.Range}{2\sqrt{2}}}{Resolution})$

[3] $FoM = \frac{Power*Meas.Time}{2^{ENOB}}$

Figure 27.7.6: Performance summary and comparison.

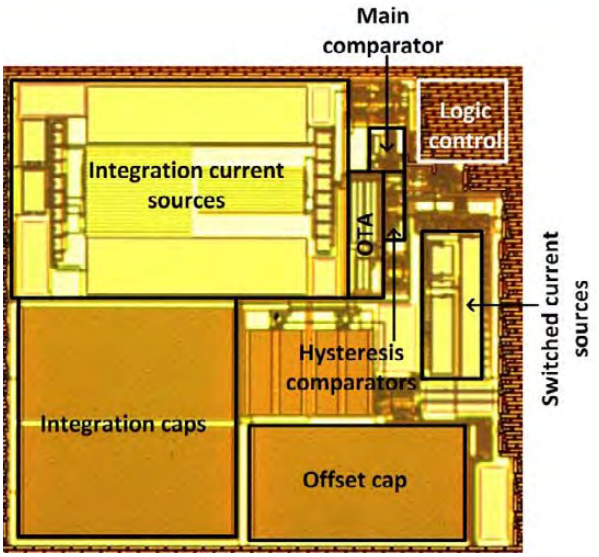

Figure 27.7.7: Chip micrograph.

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