27.5 A 30ppm <80nJ Ring-Down-Based Readout Circuit for Resonant Sensors

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Resonant sensors are a promising candidates for energy-constrained applications. For instance, the resonance frequency shift of polymer-coated MEMS resonators has been used to realize electronic nose systems for personalized health and environmental sensing [1]. Oscillator-based readout circuits for such sensors have been successfully implemented [2,3], but are relatively power-hungry, difficult to design in the presence of parasitic capacitance, and only provide information about the resonance frequency, f_{res}, while the quality factor, Q, often includes additional valuable information.

As an alternative, measurement of the ring-down transient of a resonator can be used to determine both f_{res} and Q. This approach is less sensitive to parasitics and potentially much more energy-efficient. However, prior integrated realizations of this technique require three or more ring-downs to obtain information about both f_{res} and Q [4,5], while this information can, in principle, be obtained from a single ring-down, and thus at significantly lower energy consumption. This paper presents an integrated readout circuit capable of doing this (Fig. 27.5.1). The circuit has been optimized for use with SiN piezo-actuated clamped-clamped beam resonators [1], whose near-resonance impedance can be modeled as an RLC tank shunted by a capacitor, C_p, which models the capacitance of the transducer plus parasitics.

The circuit operates as follows. During an excitation phase, ϕ_{exc}, it drives the resonator using an excitation signal, V_{drive}, at a frequency close (but not necessarily equal) to f_{res}, so that energy is added to the resonance mode of the sensor. Then, during a ring-down phase, ϕ_{ring}, the excitation stops. The resonator continues to oscillate at f_{res}, producing an exponentially decaying current, which is turned into voltage V_{ring} by a transimpedance amplifier (TIA).

To determine Q from the envelope of V_{ring}, a comparator detects the number of level crossings of V_{ring} at a threshold voltage, V_{thld}, that is dynamically adjusted during ring-down by a capacitive DAC (CDAC). Initially, a high threshold is used, which is switched back in three steps to a level that corresponds to the steady-state level of V_{ring} (Fig. 27.5.2). This switching happens when the envelope of V_{ring} drops below the threshold level, so that the number of level crossings counted up to that point (N_1, N_2 and N_3) is a measure of the time at which the envelope reaches the corresponding threshold level. From these counts and the ratios of the threshold levels, an estimate of the time constant of the decay, and thus of Q, can be obtained. In order to determine f_{res}, counting continues until a pre-defined number of N_{total} ring-down cycles has been reached. This happens a time $T = N_{total} / f_{res}$ after the start of the ring-down. Hence f_{res} can be obtained from T, which is quantized by an additional counter that counts the number of clock cycles of a reference clock, *clk*, during this time period.

To decide when to switch the threshold to the next level, a time-out mechanism is employed. A timer continuously checks the time passed since the last level crossing. If this exceeds a time-out period, the envelope is assumed to have dropped below the threshold level. The threshold is then switched (briefly) to V_{cm}, to ensure that a next level crossing will be found, and then to the next threshold level. The time-out period is set roughly equal to one cycle of the ring-down signal by employing the same timer during the first cycle of the ring-down to obtain a rough estimate of the duration of one cycle.

For current efficiency, the TIA is implemented around a cascoded inverter-based OTA [6], while the comparator employs a two-stage inverter-based topology with a class-AB output stage. Their combined offset voltage is critical, as it determines the difference between the final threshold level and the steady-state level of the ring-down signal, and hence limits how many zero crossings can be detected. Therefore, a two-step auto-zeroing (AZ) scheme is used prior to the excitation phase, similar to that of [5] (Fig. 27.5.3). During phase ϕ_{AZ}, the OTA is auto-zeroed to set its bias point and store its input offset on a capacitor, C_{AZ}. During phase ϕ_{AZC}, similarly, the first stage of the comparator is auto-zeroed, storing its input offset on C_{AZC}. Phase ϕ_{AZ} ends first, so that any residual output offset of the OTA will be corrected by the auto-zeroing of the comparator.

During the subsequent phase, ϕ_{exc}, the resonator is disconnected from the TIA and driven by an on-chip driver, which is clocked by an off-chip generator set to a fixed frequency close to f_{res}. The driver alternately pulls V_{drive} to ground and to a reference voltage using a source follower. After ϕ_{exc}, the resonator is reconnected to the TIA, which is held in unity-gain during a short phase ϕ_{Cp}. This quickly discharges the resonator parasitic capacitance, C_p, to the virtual ground of the OTA, preventing any charge that may have been left on C_p at the end of ϕ_{exc} from causing an undesired transient at the TIA output. The TIA output is capacitively coupled using C_C to the input of the comparator, as are the binary-weighted capacitors of the 3b CDAC, which are driven using logic levels $D_{1,2,3}$. During auto-zeroing, the CDAC inputs are zero. During the ring-down phase, they are switched, changing the voltage stored on C_C via charge-redistribution, and thus effectively changing the threshold of the comparator as desired.

The readout circuit is implemented in a 0.35µm CMOS process, occupies an active area of 0.24mm^2 (Fig. 27.5.7), and consumes 34µA from a 1.8V supply. The chip includes all analog circuits, as well as the period time-out detector. The control signal generator and counters have been implemented in an off-chip FPGA for flexibility. To accommodate various resonator characteristics, the TIA feedback network has been made reconfigurable. The chip has been tested in combination with three different resonators with f_{res} = 469 kHz, 537 kHz, 592 kHz and Q = 521, 386, 376 (under ambient conditions).

To illustrate the frequency resolution, Fig. 27.5.4 shows the standard deviation of f_{res} as a function N_{total}, which determines the measurement time. For smaller values of N_{total}, the resolution is limited by quantization errors introduced by the counter. For larger values, jitter of the comparator output starts to dominate. An optimum better than 30ppm is reached for all three resonators for $N_{total} \cong Q$, which corresponds to a total measurement time of less than 1.3ms (including the excitation phase). To demonstrate the combined measurement of f_{res} and Q, the resonators have been exposed to different pressure levels in a vacuum chamber, which produces significant variation in Q due to changing air damping, as well as a smaller variation in f_{res}. Figure 27.5.5 shows the f_{res} and Q measured using the chip along with the corresponding values measured using a bench-top impedance analyzer (Agilent 4294A). The two sets of measurements are in close agreement, demonstrating the effectiveness of the readout circuit.

Figure 27.5.6 summarizes the chip performance and compares it to previously published readout circuits for similar resonators. Oscillator-based readout circuits for a similar resonator [2,3] achieve similar or better resolution, but at much higher power and much longer measurement time, and without providing information about Q. In contrast with earlier ring-down based designs [4,5], this work only requires a single ring-down to measure both f_{res} and Q. Moreover, with a similar resonator to that in [5], it achieves 1.6× better resolution at 7.8× less energy consumption. These characteristics make the presented circuit a promising candidate for use in energy-constrained sensing applications.

Acknowledgements:
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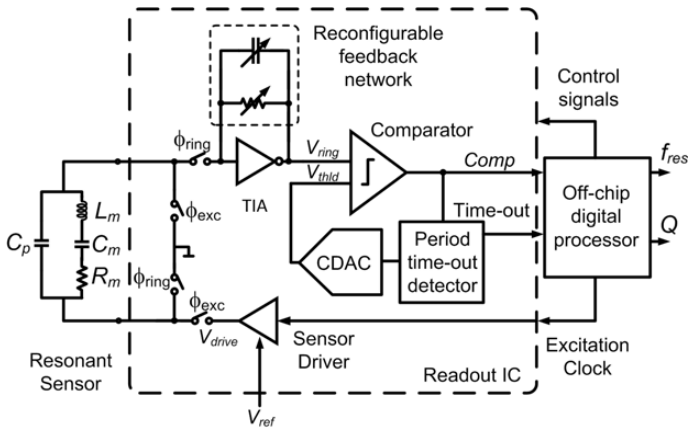

Figure 27.5.1: Block diagram of the ring-down-based readout circuit.

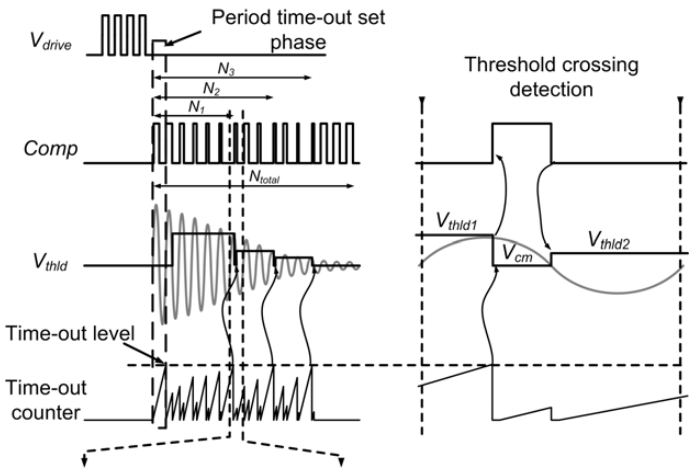

Figure 27.5.2: Timing diagram of one ring-down measurement.

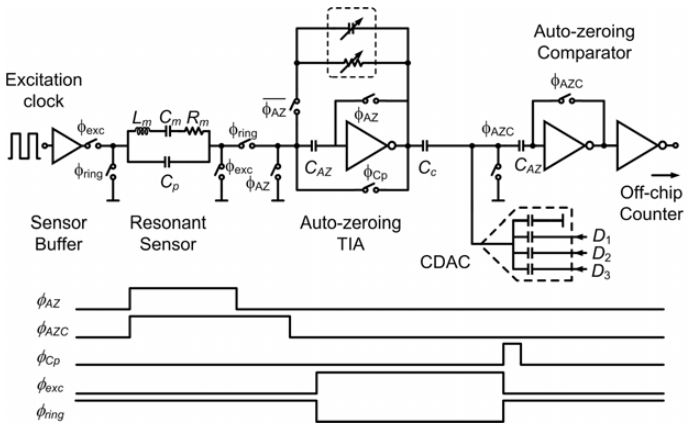

Figure 27.5.3: Circuit diagram of the readout, with associated timing diagram.

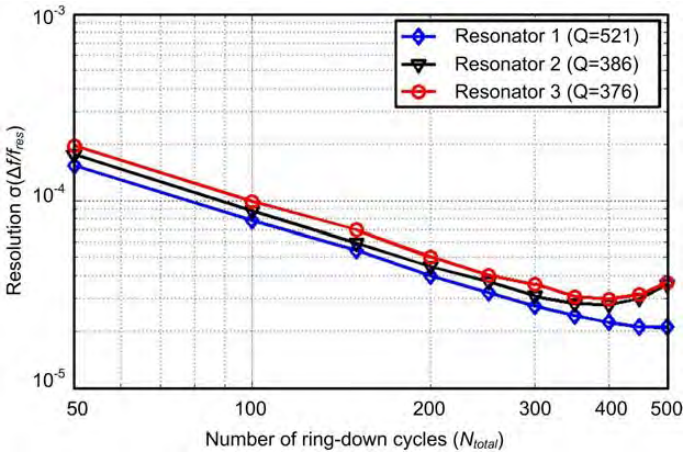

Figure 27.5.4: Measured resolution of f_{res} as a function of N_{total}.

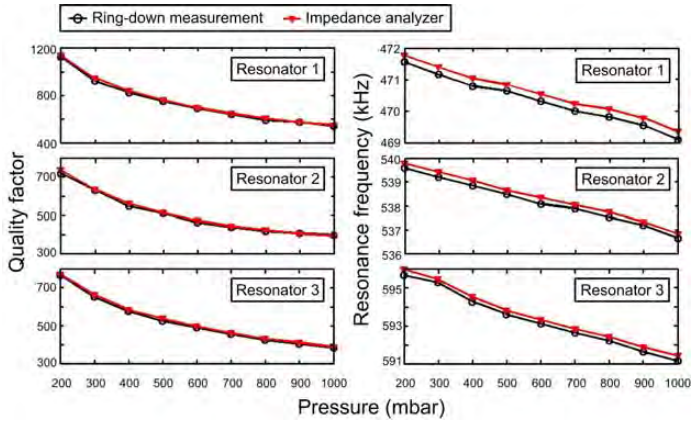

Figure 27.5.5: Measured frequency and quality factor shift associated with different pressure levels.

Parameter	Petrescu [2]	Pettine [3]	Zeng [4]	Yan [5]	This work		
Technology	0.25µm CMOS	0.25µm CMOS	0.35µm CMOS	0.35µm CMOS	0.35µm CMOS		
Supports Q measurement	No	No	Yes	Yes	Yes		
Supply voltage (V)	3.3	3.3	3.3	3.3	1.8		
Supply current (µA)	409	409	36	31.5	34		
Resonance freq. (kHz)	1980	2170	2010	535.8	469	536	592
Quality factor	280	450	667	386	521	386	376
Conversion time (ms)	5000	10000	3	6	1.3	1.2	1.1
Resolution (ppm)	27	2.4	250	50	21	27.7	29.8
Energy per meas (µJ)	6748.5 [1]	13497 [1]	0.356 [2,3]	0.624 [2,3]	0.080 [2]	0.073 [2]	0.067 [2]

[1] Excludes frequency counter; [2] excludes counter and signal generator; [3] excludes sensor driver

Figure 27.5.6: Performance summary and benchmarking.

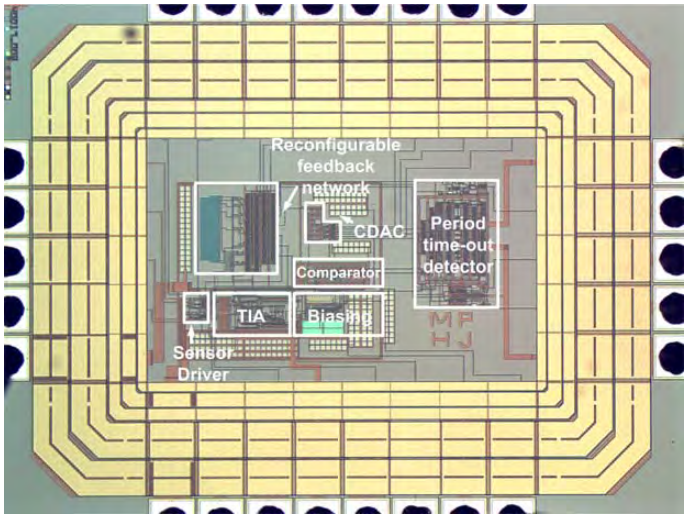

Figure 27.5.7: Chip micrograph.

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