27.2 A 1.2μg/√Hz-Resolution 0.4μg-Bias-Instability MEMS Silicon Oscillating Accelerometer with CMOS Readout Circuit

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Inertial navigation sets a very stringent requirement on the long-term stability of an accelerometer, which is characterized by bias instability. Long-term stability demands a very low-noise design. Accelerometers based on capacitance sensing are the mainstream MEMS accelerometers reported recently [1-3]. The state-of-the-art achieves 1μg bias instability and 2μg/Hz$^{1/2}$ resolution with a full scale of ±15g [1]. Compared with capacitive accelerometers, a MEMS silicon oscillating accelerometer (SOA) has the advantage of large input dynamic range and has potential to achieve better performance. So far, only a few SOAs with CMOS readout circuits have been reported. Among them, the best performance metrics achieved are 4μg bias instability and 20μg/Hz$^{1/2}$ resolution [4].

This paper demonstrates a MEMS SOA with superior performance. Fig. 27.2.1 shows the system block diagram of the SOA. Two identical CT readout channels form two oscillators with MEMS resonators, respectively. When subject to input acceleration, the two oscillation frequencies change in opposite directions and their difference is a measure of the acceleration. An on-chip digital frequency measurement circuit measures the output frequencies of each oscillator and converts them to digital outputs. Each oscillator consists of a MEMS resonator connected to a proof mass, a front-end amplifier, an automatic amplitude control (AAC) circuit and a variable gain amplifier (VGA). The front-end senses and amplifies the motional current from the MEMS resonator, and generates two outputs that are proportional to displacement and velocity of the vibrating beam, respectively. The velocity signal is fed back to drive the MEMS resonator through the VGA to meet the phase requirement. The AAC loop precisely controls the amplitude of the displacement signal to prevent the MEMS resonator from entering a strong nonlinear region. Several circuit techniques are employed in the AAC loop to suppress flicker noise that can severely deteriorate phase noise through the amplitude-stiffness (A-S) effect. The frequency measurement circuit contains waveform reshaping, a PLL and a frequency-to-digital converter (FDC). The 25kHz analog signal is converted to square wave by waveform reshaping, and then boosted to 3MHz by a low-power PLL, which also performs as a band-pass anti-aliasing filter to facilitate subsequent FDC.

The challenge in the SOA readout circuit, apart from the low-noise front-end, is the AAC loop. It needs to be carefully designed to suppress flicker noise, which transforms into amplitude noise after being modulated by the velocity signal in the VGA and causes oscillation frequency fluctuation through the A-S effect. In [4], a chopper technique is applied to the amplitude detector and subtractor to remove flicker noise. In this work, we found that other noise sources in the AAC loop, such as that in the buffer, should also be minimized. In addition, a conventional chopper or auto-zero technique removes only additive flicker noise, but leaves multiplicative flicker noise, such as that present in a tail current source, unsuppressed. This is because the multiplicative flicker noise affects the gain and is effectively modulated to the chopper frequency. Hence, it will appear in the signal band after the second chopper.

Figure 27.2.2 shows the AAC circuit implementation. The buffer is an OTA followed by a source follower to provide a DC shift. The noise from MN3 and MN4 affect the gain of MN1 and MN2, and generate multiplicative noise. However, they are attenuated by series-shunt feedback (C2) and source degeneration. The amplitude detector uses an alternative-voltage-follower (AVF) and it also only generates additive noise as the multiplicative noise from MP1 is suppressed by source degeneration feedback. The voltage-to-current (V-I) converter in the subtractor converts the detected amplitude to current and the subtraction with an external V_{REF} is subsequently done in the current domain. In a conventional V-I converter where a tail current is employed, the noise in MN7, MN8 and MN11 affect the trans-conductance (g_m) and hence generate multiplicative noise. Though the source degeneration resistor (R_s) can help reduce gain dependence on g_m, it requires g_m to be much larger than $1/R_s$, which leads to large power overhead. The proposed subtractor in Fig. 27.2.2 utilizes a low-power OTA and a series-shunt feedback to boost the open loop gain, which makes the effective closed-loop trans-conductance $R_2/(R_1 \cdot R_s)$ and independent of g_m. Thus, the multiplicative noise from MN12, MN13, MN14 and MN15 will not appear at the output. In this design, a chopper is employed in all the above three blocks to remove remaining additive flicker noise, as shown in Fig. 27.2.1.

The front-end shown in Fig. 27.2.3 is essentially a band-pass trans-impedance amplifier. It consists of an integrator, followed by a differentiator to provide an output proportional to the velocity to drive the MEMS resonator. The measured performance of front-end TIA is shown in Fig. 27.2.4. It provides a gain of 45MΩ and bandwidth of 350kHz. The phase shift at the 25kHz signal frequency is less than 2.5°. Meanwhile, it achieves 6.7fA/Hz$^{1/2}$ input-referred current noise, while consumes only 583μW. The VGA is also shown in Fig. 27.2.3. The bottom transistors that are driven by loop filter outputs operate in the linear region and act like source-degeneration resistors. The VGA can tolerate a large input swing of V_c, which occurs at oscillator start-up, and thus shortens the start-up time. The output of the VGA directly drives the MEMS resonator.

The FDC, shown in Fig. 27.2.3, is based on similar concept in [5]. The phase of the input signal is quantized by a 4b counter. The value is then subtracted from a register that stores the previous value. This behaves like a first-order difference ($1-z^{-1}$). As a result, the output digital code represents the frequency reading, and it has inherent first-order noise shaping. The quantization noise is below the white phase noise of the SOA analog output so that the performance of the SOA is not limited by the FDC. This requires the sampling frequency to be higher than 24MHz. The measured frequency deviation of a 25kHz input signal from a signal generator and the corresponding noise spectrum are plotted in Fig. 27.2.4.

Figure 27.2.7 shows the structure of the MEMS sensor, consisting of two resonators linked to a proof mass. This differential topology not only increases the scale-factor, but also cancels the correlated noise and temperature drift between the two resonators. For each resonator, two pairs of differential comb-shaped capacitors are arranged for continuous driving and sensing, while the double-ended tuning fork (DETF) is connected at the center to achieve fully differential operation [4]. The MEMS sensor is fabricated in an 80μm thick SOI process with a wafer-level vacuum package. The intrinsic resonant frequency of each resonator is designed to be 25kHz and the scale factor is 260Hz/g. The quality factor of the resonator is around 30000. With a centrifugal test, the full scale of the SOA is ±20g with a nonlinearity of 166ppm.

The performance of the SOA is measured from the analog outputs. The bias instability and resolution are obtained from Allan variance in the time domain and noise spectrum density in frequency domain, respectively. The SOA achieves 0.4μg bias-instability and 1.2μg/Hz$^{1/2}$ resolution, as shown in Fig. 27.2.5. The whole chip consumes 4.37mW under a 1.5V supply. Table in Fig. 27.2.6 gives the performance summary and comparison with both state-of-the-art SOAs and capacitive accelerometers. The readout circuit is implemented in a 0.35μm CMOS process and occupies 6mm^2. The micrograph of the chip together with the MEMS sensor is shown in Fig. 27.2.7.

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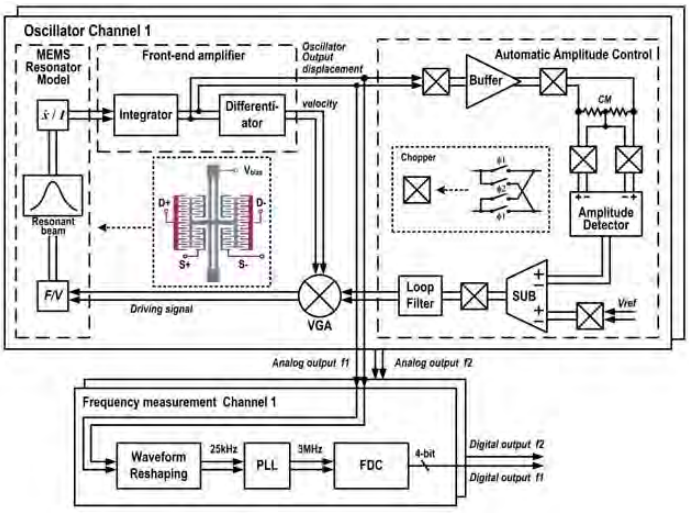

Figure 27.2.1: SOA system block diagram.

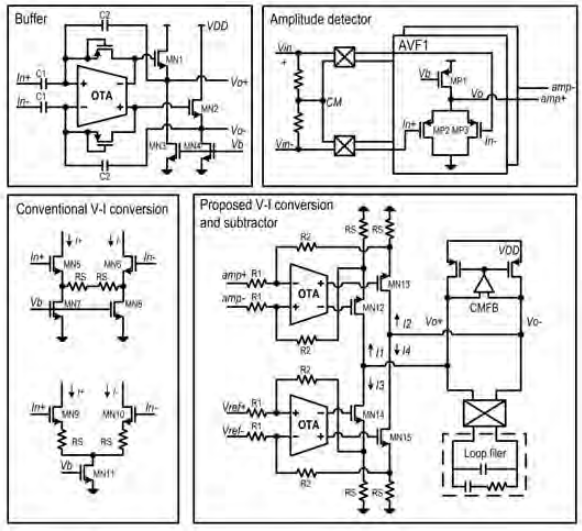

Figure 27.2.2: Simplified schematics of the AAC loop (some choppers are omitted).

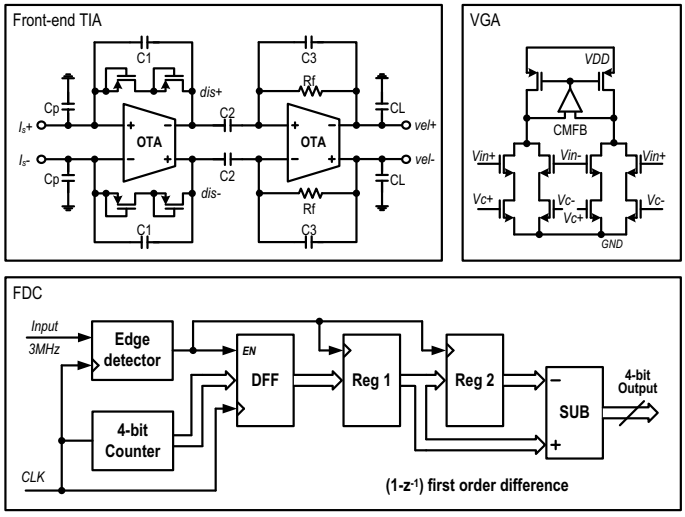

Figure 27.2.3: Simplified schematic of front-end TIA (top-left), the VGA (top-right) and the FDC (bottom).

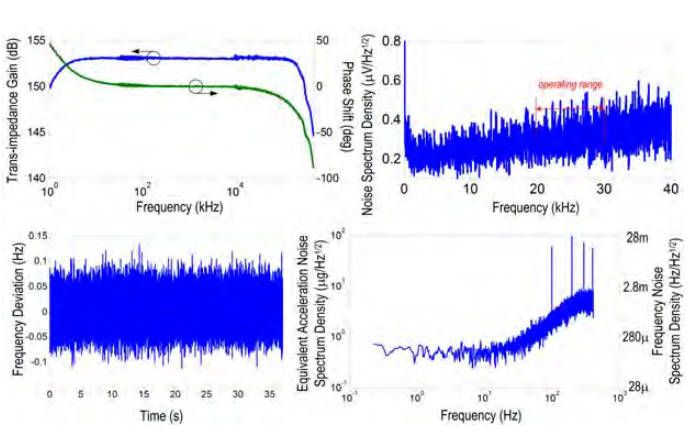

Figure 27.2.4: Measured frequency response and output noise spectrum density of front-end TIA (top); measured performance of the FDC (bottom): frequency deviation (decimated to 820Hz) of a 25kHz input and noise spectrum in terms of frequency and equivalent acceleration.

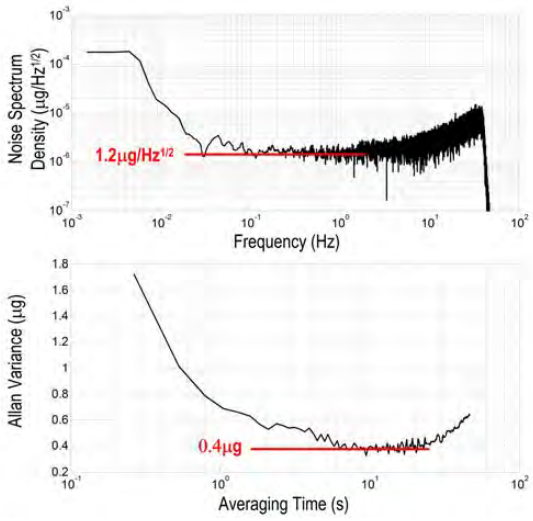

Figure 27.2.5: Measured acceleration resolution and bias-instability of the SOA.

Parameter	[1]	[2]	[3]	[4]	This work
Mechanism	Capacitive	Capacitive	Capacitive	SOA	**SOA**
Process(μm)	NA	0.35	0.5	0.35	**0.35**
Supply (V)	NA	3.6	3	3.3	**1.5**
Full scale (g)	±15	±1.15	±0.5	±20	**±20**
Power (mW)	100	3.6	4.5	23	**4.37**
Bias instability (μg)	1	13	8	4	**0.4**
Resolution (μg/Hz1/2)	2	2	4	20	**1.2**
Readout	Σ–Δ	Σ–Δ	Σ–Δ	SC	**CT**

Figure 27.2.6: Performance summary and comparison with prior art (MEMS accelerometers).

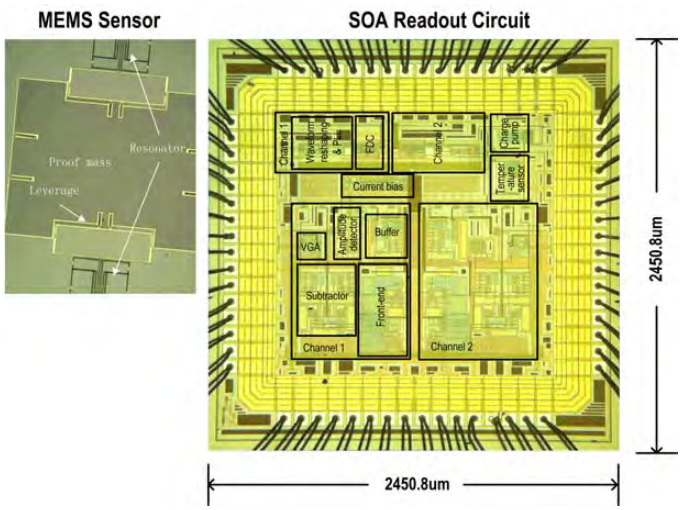

Figure 27.2.7: MEMS sensor and ASIC readout chip micrographs.

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