

27.1 A 3-Axis Gyroscope for Electronic Stability Control with Continuous Self-Test

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Gyroscopes and accelerometers form the core of Electronic Stability Control (ESC) systems [1], which are mandated for new vehicles in many countries. Gyroscopes for ESC applications require higher performance specifications than those of consumer gyroscopes available in the market today. In addition, they require continuous safety monitoring so that changes in the output, which happen in the field due to MEMS and circuit malfunctions, are flagged and are not misconstrued for legitimate signals. This work presents a low-overhead approach for implementing accurate continuous safety monitoring by augmenting the function of already existing sub-systems. In addition, the paper discusses circuit architecture and design techniques, which achieve the stringent ESC specifications for noise, robustness to parasitic resonant modes in the sensor element and offset drift due to temperature and Electro-Magnetic Interference (EMI).

Figure 27.1.1 shows a block diagram of the 3-axis gyroscope for Bosch's Electronic Stability Program (ESP®). The three detection channels sense yaw, roll and pitch rotation rates. The device is actuated by a single drive channel. The Coriolis detection is done by a closed force-feedback loop (Fig. 27.1.2), which applies a restoring force to counter the Coriolis force and maintains the proof mass near its center position along the particular Coriolis detection axis. The same set of electrodes is used for capacitive sensing and force-feedback enabling collocated control, which improves the stability of the system [2]. The high quality factor of the sense channel mechanics, ranging from hundreds to a thousand, provides the necessary loop gain. This eases the noise requirement for the Capacitance-to-Voltage (C/V) converter and the ADC shown in Fig. 27.1.2. The unwanted quadrature force on the moving mass is cancelled electro-mechanically using the quadrature cancellation loop. Cancellation of the quadrature motion results in an improved offset performance.

ESC systems require the highest automotive safety standard, ASIL-D [3]. All circuit blocks need to be continuously monitored and deactivated when readings fall outside certain limits. The traditional approach of monitoring the outputs of a large number of circuit blocks incurs a sizeable area penalty. To overcome this inefficiency, we inject two test signals (Fig. 27.1.2) and measure the response of the system after they traverse the entire signal path with a certain known gain. Using two signals at different frequencies provides redundancy. The presence of the sub-system for cancelling the quadrature error of the gyroscope provides a convenient way for introducing the test signals with minimum circuit overhead and minimum interference with the desired signal. Injecting the test signals in the quadrature channel makes them immune to Coriolis rate signals at the same frequencies since the Coriolis and quadrature signals are 90° out of phase and can be separated. A certain pre-specified change in the magnitude of these signals would indicate a failure. This approach reduces the number of monitors required by more than a factor of 10, thereby reducing algorithm complexity and chip area for detecting failures. The test tones are located at frequencies of approximately 700Hz and 1200Hz. The frequencies are chosen so that the inter-modulation products of the tones, due to various non-linearities in the MEMS, fall outside the signal band of interest, while the tones themselves fall inside the bandwidth of the Coriolis detection channel. The amplitude of each tone, referred to the Coriolis rate, is chosen as 100°/s so that a 5% change in its magnitude is large enough compared to the noise floor and is detected within 20ms. The full-scale range of the Coriolis signal is 630°/sec. Fig. 27.1.2 also illustrates the mechanism through which the phase noise skirts around the test tones appear inside the frequency band of interest, thus increasing the noise floor. The modulation of phase noise happens in the feedback DAC (Digital-Force Converter) of the Coriolis detection loop. This loop can be viewed as a continuous-time $\Delta\Sigma$ modulator, which is well known to be susceptible to clock jitter [4].

Figure 27.1.3 shows the drive loop, operating at the resonant frequency (f_0) of 25kHz, with the PLL embedded in it. To reduce the jitter-induced noise degradation in the Coriolis detection loop, we need to minimize the phase noise of the 400kHz clock (f_{clk}) around the test tone frequencies of approximately 700Hz and 1200Hz. The phase noise at these frequencies is mainly due to the

band-pass (BP) $\Delta\Sigma$ ADC and the VCO $\Delta\Sigma$ modulator in the drive loop of Fig. 27.1.3. The BP $\Delta\Sigma$ ADC has two integrators forming a resonator and a summing amplifier, which sums the resonator output with the feed-forward input from the first integrator. A step voltage is applied to the proof mass to sense its displacement through the drive detection capacitors. Since the interface IC is designed to work with a wide variety of sensors, the frequency of the step voltage is limited to 400kHz, based on the worst-case parasitics of the sensor variants. The noise of the ADC around 25kHz translates to the close-in phase noise of the clock. With the ADC's clock frequency limited to 400kHz, the ADC feedback path uses a 5b capacitive DAC to reduce the quantization noise to acceptable levels. Dynamic Element Matching (DEM) is not used for this DAC since mismatch results in negligible noise increase at the test tone frequency offsets. A 5b split-capacitor array SAR ADC clocked at 6.4MHz serves as the quantizer for the ADC.

The PLL loop filter is clocked at 400kHz since the data coming from the ADC is at that rate. The 3rd order digital $\Delta\Sigma$ modulator which drives the VCO DAC is, however, clocked at 6.4MHz in order to shape the quantization noise to higher frequencies. The VCO DAC is implemented using a 4-tap FIR filter to reduce the degradation of its output due to clock jitter (Fig. 27.1.3). The amplitude control loop is a narrow-band loop with 100Hz bandwidth. It has a Proportional-Integral (PI) controller followed by a 2nd order 4b $\Delta\Sigma$ modulator, whose output controls the gain of a pseudo-sinusoidal DAC. The current from this DAC flows into a high voltage amplifier, which drives the MEMS actuation capacitors.

The digital PLL also acts as a narrow-band filter and prevents the drive loop from locking to parasitic mechanical resonant modes. Further, the simple pseudo-sinusoidal DAC with element values of 1x, 2x, 3x and 4x drives the MEMS proof mass with steps approximating a sinusoid (Fig. 27.1.3). Compared to a square wave, this waveform has lower harmonic content and therefore reduces the chance of exciting parasitic modes. Thus, the use of the PLL and a pseudo-sinusoidal DAC significantly reduces the chance of the drive loop locking to an undesired resonant mode.

The 3-axis gyroscope sensor interface circuit is implemented in a 130nm high-voltage CMOS process. The readout circuits, along with the references, LDOs, decoupling capacitors and charge pumps occupy 2.3mm² and consume 8.8mA from a 3V supply. The digital portion of the prototype is implemented in an FPGA for reasons of flexibility. The mechanical sensor element is fabricated in the Bosch surface-micromachined MEMS process with a 20 μ m structural poly-Si layer.

Figure 27.1.4 shows the measured output spectrum of the Coriolis detection loop (400kHz rate) before demodulation to baseband. The two test tones are seen modulated around the 25kHz drive frequency. The noise floor across an 80Hz bandwidth is 0.0039°/s/ $\sqrt{\text{Hz}}$ with the test tones and 0.0038°/s/ $\sqrt{\text{Hz}}$ without the test tones. Thus, the phase noise skirts around the test tones causes negligible increase of the noise floor. The close-in double side band (DSB) phase noise for the 400kHz clock is -77dBc/Hz up to the PLL bandwidth of 1.8kHz.

Figure 27.1.5 shows the offset drift performance with respect to temperature and EMI. The offset drift (without temperature compensation) is less than $\pm 0.1^\circ/\text{s}$ over the automotive temperature range of -40 to 140°C. EMI is characterized under an electric field of 1200V/m peak-to-peak in a frequency range from DC to 2.5MHz in steps of f_0 . EMI-related degradation comes primarily from the electric field coupling onto bond wires at frequencies of $N \times f_{clk} \pm f_0$ ($N=1,2,\dots$). The maximum EMI-induced error is 1.2°/s. The effect of EMI is not pronounced due to the attenuation provided by the high-Q of the sensor element. The root Allan variance of the output angular rate is 1.2°/hr (Fig. 27.1.6).

Acknowledgements:

The authors would like to thank M. Roczniak, B. Kuhlmann and R. Schillinger for their help during the project.

References:

- [1] J. Marek, "MEMS for Automotive and Consumer Electronics", *ISSCC Dig. Tech. Papers*, pp. 9-17, Feb. 2010.
- [2] V. Petkov, *et al.*, "A Fourth-Order SD Interface for Micromachined Inertial Sensors", *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1602-1609, 2005.
- [3] ISO 26262: Road Vehicles-Functional safety, http://www.iso.org/iso/catalogue_detail?csnumber=43464
- [4] K. Reddy, *et al.*, "Fundamental Limitations of Continuous-Time Delta-Sigma Modulators Due to Clock Jitter", *IEEE Trans. on Circuits Systems-I*, vol. 54, no. 10, pp. 2184-2194, 2007.

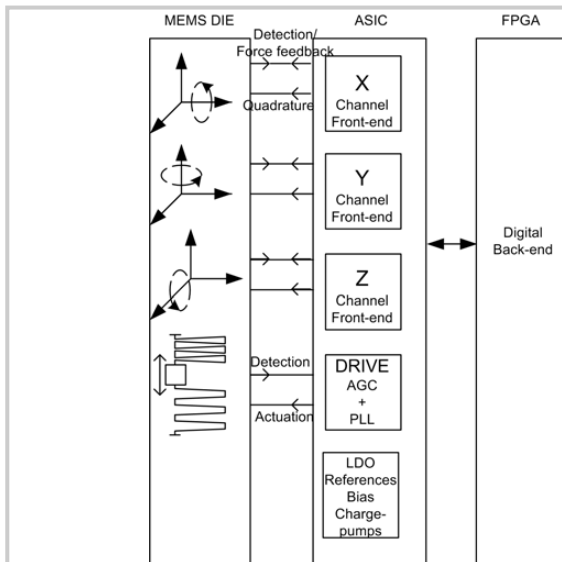


Figure 27.1.1: System block diagram.

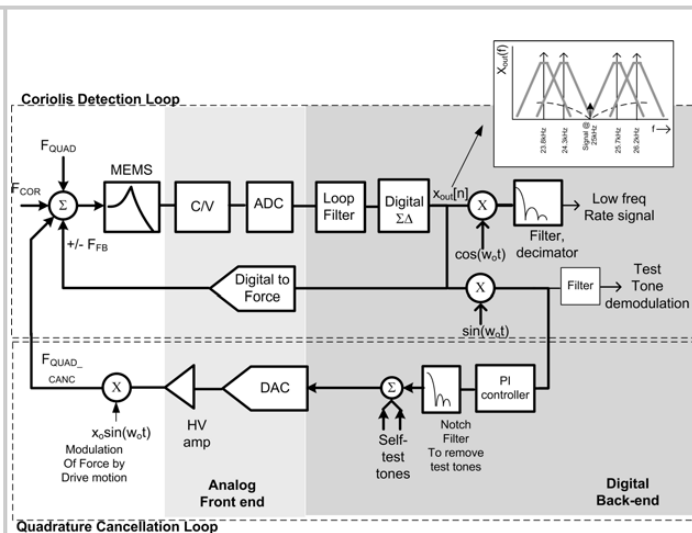


Figure 27.1.2: Coriolis detection and quadrature cancellation loops.

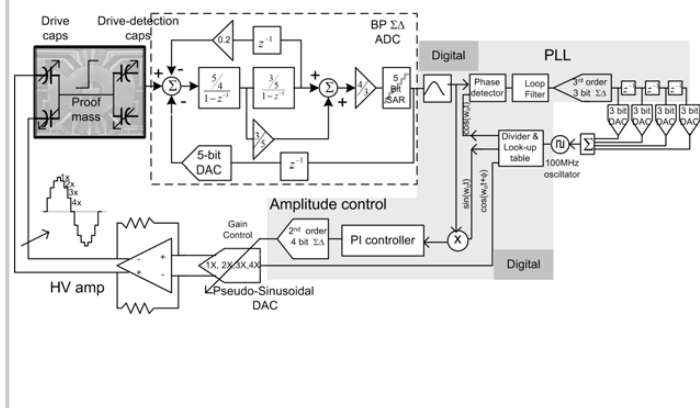


Figure 27.1.3: The Drive PLL and amplitude control loops.

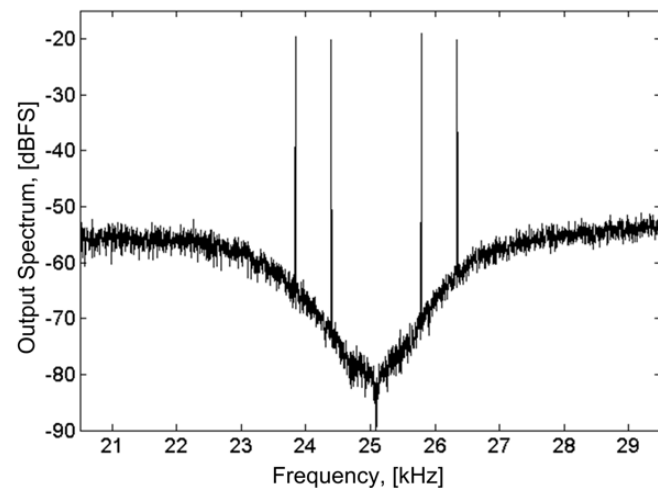


Figure 27.1.4: 400kHz measured spectrum of the output of the Coriolis detection loop with test tones.

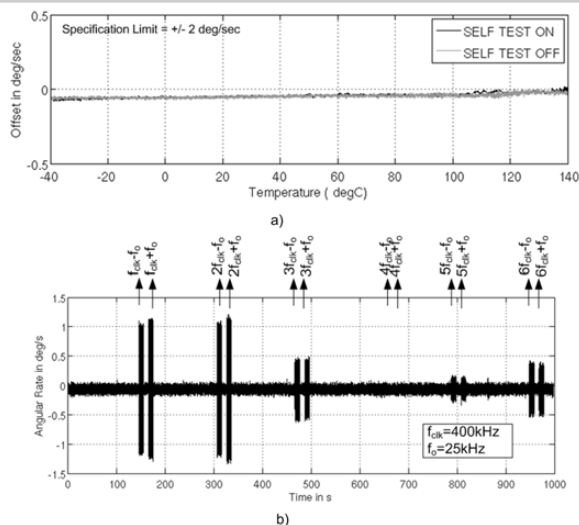


Figure 27.1.5: Measured offset drift with respect to a) temperature (without temperature compensation), and b) frequency of EMI.

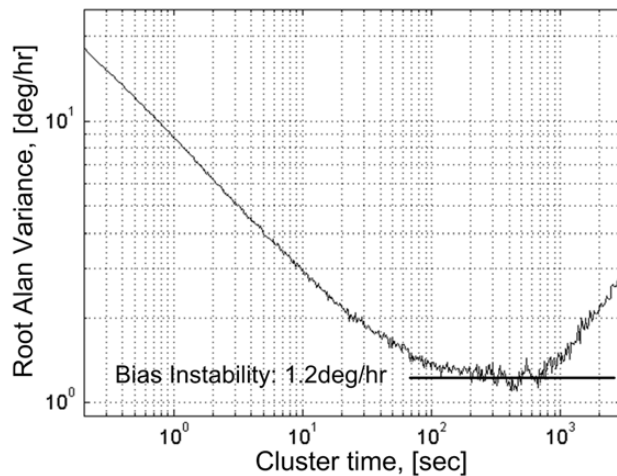


Figure 27.1.6: Measured root Allan variance of the Coriolis signal.

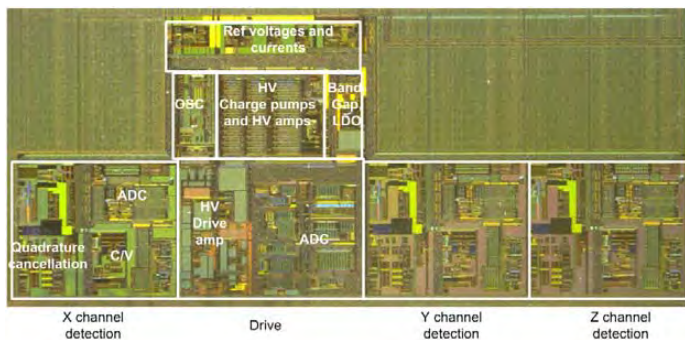


Figure 27.1.7: Chip photograph.