26.7 A 2.6b/cycle-Architecture-Based 10b 1.7GS/s 15.4mW 4×-Time-Interleaved SAR ADC with a Multistep Hardware-Retirement Technique

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With the growing interest in time-interleaved (TI) structures, the conversion rates of ADCs have greatly improved, which has inevitably increased power consumption. Despite the advantages of TI structures, power consumption is increased due to the stricter matching requirements between channels; in some cases, >50% of total power is for calibration purposes [1]. Thus, to realize high-speed and high-resolution ADCs with TI structures, it is important to alleviate the calibration burden by choosing a suitable number of power-efficient high-speed single channels. Previously reported CDAC-based 2b/cycle structures [2-5] made contributions in realizing high-speed single-channel ADCs [2-4] with high resolution [5] by using additional capacitive DACs and modified switching logic. The power overhead and the complexity of the additional logic and DACs for 2b/cycle implementations have been of trivial concern for low resolution ADCs. However, as resolution increases, the complexity of such circuits becomes considerable, with power taking up a big share of the total. In this paper, a multi-step hardware-retirement (MSHR) technique, which disables low-accuracy hardware blocks of scaled sizes with the requirement relaxations from redundancies in an advancement to the reconfiguration scheme in [5], is reported to alleviate the overhead of additional logic and DACs for ADCs, requiring high resolutions. A low-power 2.6b/cycle-based SAR ADC architecture is presented as a proof of concept.

Figure 26.7.1 shows a block diagram of the single-end equivalent 10b SAR ADC with 2.6b/cycle architecture. The SAR ADC includes three DACs (SIG-DAC, REF-DAC1, REF-DAC2) and five comparators (CMP0-4). The sizes of REF-DAC(1,2) are designed to be 1/4 of SIG-DAC, while those of CMP(0,1,3,4) are set to be 1/4 of the CMP2, respectively, thanks to the implementation of the MSHR technique with redundancies. The overall sizes of DACs and comparators are 1.5 and 2 times the sizes of SIG-DAC and CMP2, respectively, making the hardware compact. REF-DAC(1,2) form decision thresholds for code decisions independent of the input. The capacitor switching operations of REF-DAC(1,2) are merged with the reference switches shared between REF-DAC1 and REF-DAC2, as shown in Fig. 26.7.1 to simplify control logic. Unlike the REF-DAC, SIG-DAC samples the input and forms a residue after each bit decision. Note that only one SIG-DAC is employed, making the complexity of input-dependent control logic comparable to that of conventional 1b/cycle architectures. A total of 12 cycles are used for a complete single-channel SAR bit decision, where 4 cycles are allocated for sampling purposes. Within the 4 sampling cycles, only 3 cycles are used for pure sampling, while 1 cycle is used to reset SIG-DAC to alleviate the burden of the input driver and to improve sampling linearity.

Figure 26.7.2 shows a schematic of SIG-DAC and a descriptive table of the overall structure. Within the total of 536C in SIG-DAC, a total redundancy of 24C is utilized, making the effective reference scale V_{REF}* equal to 512/536 V_{REF}. As shown in the table, the design performs two cycles of 2.6b/cycle decision operations with step sizes of 160 LSB and 40 LSB, two cycles of 2b/cycle operations with 16-LSB and 4-LSB steps, and four cycles of 1b/cycle operations. Figure 26.7.3 shows the fundamental conversion operations, through waveforms, of the MSHR technique. In phase P_1, five decision threshold levels formed with ±160/512 V_{REF}* and ±320/512 V_{REF}* (from REF-DAC1 and REF-DAC2) and a spontaneous level 0 from CMP2 define six distinctive decision values with a reference step size of 160/512 V_{REF}* for a 2.6b/cycle non-binary decision with 3 MSBs ($D_{13}D_{12}D_{11}$). SIG-DAC, then, shifts its outputs to the center region according to $D_{13}D_{12}D_{11}$ before the next bit decision. Similarly, in phase P_2, redundancies of ±40/512 V_{REF}* are inserted in the upper and the lower regions of the decision range, drawing a reference step size of 40/512 V_{REF}* for another 2.6b decision. After phase P_2, REF-DAC2 and CMP(0,4) are retired from operations. The following bit decisions in phase P_3 are made with a 16/512 V_{REF}* reference step size, and with ±12/512 V_{REF}* redundancies. Such redundancies of ±12 LSBs in between phases P_2 and P_3 correct errors arising from noise and hardware errors of REF-DAC2 and CMP(0,4). For an analogous reason, redundancies of ±2 LSBs are given in between P_4 and P_5, and in between P_5 and P_6 to increase robustness against errors in REF-DAC1 and CMP(1,3). Owing to these redundancies that greatly alleviate the requirements of REF-DACs and comparators (except for CMP2), the sizes of REF-DACs and comparators could be scaled down as explained with Fig. 26.7.1 (Note that the sizes of REF-DAC2 and CMP(0,4) could have been further reduced in principle over the presented design). Figure 26.7.4 shows a DAC switching energy comparison with previously reported architectures. The average DAC switching energy of our architecture is calculated to be 173.6CV^2, with the breakdown shown in the table. Noting that the DAC switching energies of previously reported 2b/cycle architectures are 2519CV^2 [2], 1156CV^2 [3], and 579CV^2 [4], our architecture shows significantly improved energy efficiency with a multi-bit/cycle scheme, even close to the 1b/cycle MCS architecture [6] of 170CV^2.

A 4-way time-interleaved ADC is implemented in a 45nm CMOS process. The clock generator designated for sampling pulses is located at the center of the core to minimize the timing skew without calibrations. The length of routing paths from the sampling clock generator to the sampling network of each channel is about 63m, while the sampling pulse is distributed symmetrically. The ADC core occupies 0.057mm^2. A total of 15.4mW of power is dissipated at 1.7GS/s conversion rate under a 1.2V supply. 400fF of total capacitance is employed for SIG-DAC, while that of REF-DAC(1,2) is 100fF. The measured peaks of DNL and INL after foreground offset calibration are +0.98/-0.72 LSB and +0.93/-0.84 LSB, respectively. Figure 26.7.5 shows the measured dynamic performance. The SNDR is kept above 55.3dB up to 1.7GS/s conversion rate for a 1MHz input, and above 51.2dB up to the Nyquist-rate input. The rms timing skew between channels is estimated to be less than 570fs from the measurements. The resulting FoMs at 1.7GS/s conversion rate are 30.4fJ/conversion-step with the Nyquist-rate input, and a peak value of 19fJ/conversion-step at a low-frequency input. Figure 26.7.6 compares the performances of the prototype and previously reported works of comparable performance. Owing to the multi-bit/cycle scheme with MSHR technique, the number of channels in our architecture is reduced with an increased single-channel conversion rate and improved power efficiency, both in digital and analog domains, so as to exhibit improved FoM performance.

Acknowledgement:
This work was partially supported by the Samsung Electronics Semiconductor Division and the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) (No. 2012R1A2A2A01047062). The CAD tools were supported by the IDEC of KAIST.

Reference:

[1] N. Le Dortz, *et al.*, "A 1.62GS/s Time-Interleaved SAR ADC with Digital Background Mismatch Calibration Achieving Interleaving Spurs Below 70dBFS," *ISSCC Dig. Tech. Papers,* pp. 386-387, Feb. 2014.
[2] Z. Cao, *et al.*, "A 32 mW 1.25 GS/s 6b 2b/step SAR ADC in 0.13um CMOS," *ISSCC Dig. Tech. Papers,* pp. 542-543, Feb. 2008.
[3] C.-H. Chan, *et al.*, "A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure*," Symp. VLSI Circuits,* pp. 86-87, 2012.
[4] H.-K. Hong, *et al.*, "A 7b 1GS/s 7.2mW Nonbinary 2b/cycle SAR ADC with Register-to-DAC Direct Control," *IEEE CICC,* 4 pages, Sept. 2012.
[5] H.-K. Hong, *et al.*, "An 8.6 ENOB 900MS/s Time-Interleaved 2b/cycle SAR ADC with a 1b/cycle Reconfiguration for Resolution Enhancement," *ISSCC Dig. Tech. Papers,* pp. 470-471, Feb. 2013.
[6] V. Hariprasath, *et al.*, "Merged Capacitor Switching Based SAR ADC with Highest Switching Energy-Efficiency," *IET Electronics Letters,* vol. 46, no. 9, pp. 620-621, Apr. 2010.

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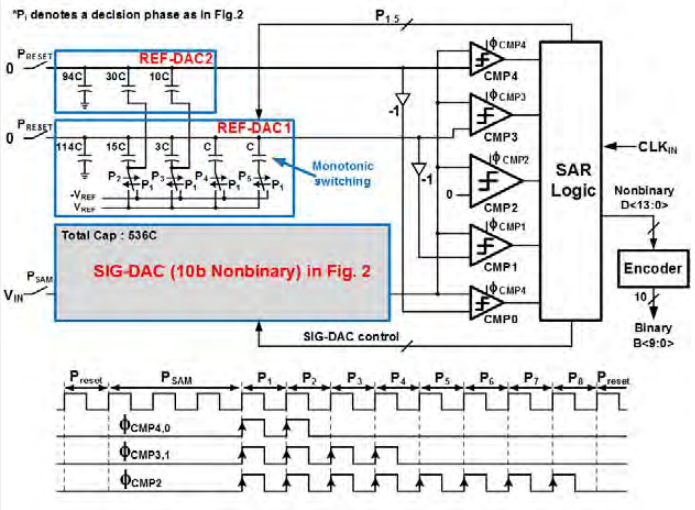
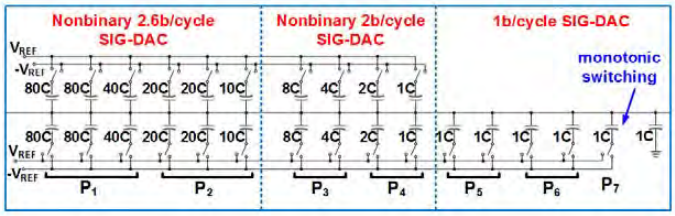


Figure 26.7.1: Block diagram and timing diagram of 2.6b/cycle 10b SAR ADC with MSHR.



Function	Sampling	Nonbinary 2.6b/cycle		Nonbinary 2b/cycle		1b/cycle				reset
Phase	P_{SAM}(3 clocks)	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_{reset}
Code Weight (LSB)	–	D_{13}: 480 D_{12}: 320 D_{11}: 160	D_{10}: 120 D_9: 80 D_8: 40	D_7: 32 D_6: 16	D_5: 8 D_4: 4	D_3: 4	D_2: 4	D_1: 2	D_0: 1	–
Circuits in use		ALL		REF-DAC1 SIG-DAC CMP1,2,3		SIG-DAC CMP2				ALL
Step size		160	40	16	4	4	4	2	1	–
Redundancy between decision phases (LSB)		±40	±12	0	±2	±2	0	0		–

Figure 26.7.2: Schematic of SIG-DAC and descriptive table of the design.

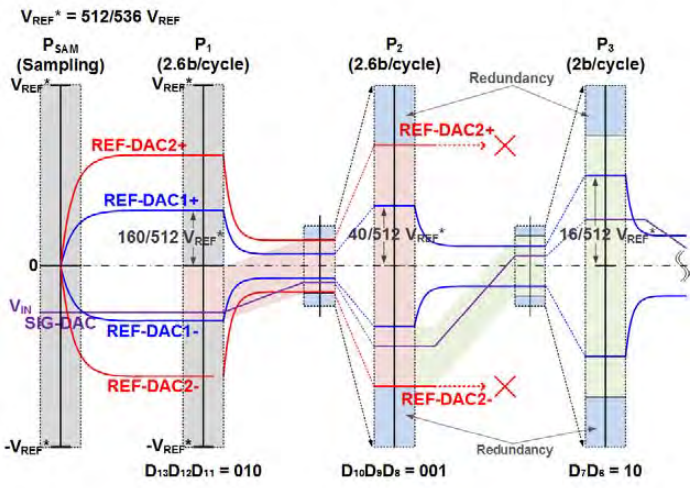


Figure 26.7.3: Design operation with MSHR and redundancies.

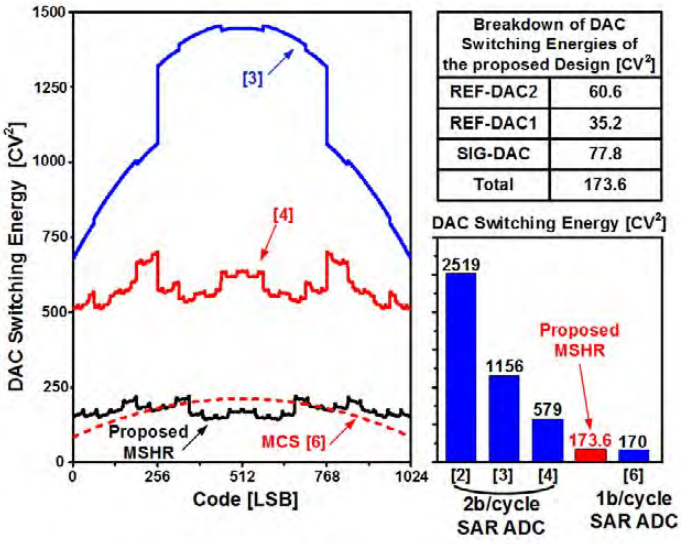


Figure 26.7.4: Comparison of DAC switching energies.

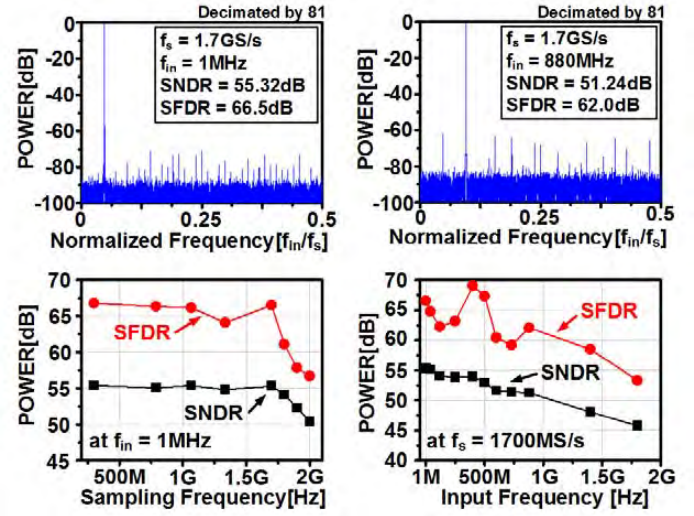


Figure 26.7.5: Measured dynamic performance.

Paper	JSSC 14, S. Hashemi	VLSI 12, B.D. Sahoo	ISSCC 14, S. Lee	ISSCC 14, N. Le Dortz	This Work	VLSI 12, D. Stepanovic
Architecture	Pipe	Pipe	SAR, TI	SAR, TI	SAR, TI	SAR, TI
Technology	65nm	65nm	65nm	40nm	45nm	65nm
Resolution	9	11	10	9	10	11
fs [MS/s]	1000	1000	1000	1620	1700	2800
Supply Voltage [V]	1.0	-	1.0	1.1	1.2	1.2
# of Channels	-	-	8	12	4	24
SNDR [dB] @Peak	51	56.3	53.3	50	55.3	50.9
SNDR [dB] @Nyquist	48	52.4	51.4	48.0	51.2	48.2
Power [mW]	7.1	32.9	18.9	93.0	15.4	44.6
FoM @Low [fJ/conv.step]	24.5	61.6	50.0	222.2	19.0	55.6
FoM @Nyquist [fJ/conv.step]	34.6	96.6	62.3	279.7	30.4	75.8
Area [mm²]	0.1	0.225	0.78	0.83	0.057	0.18

Figure 26.7.6: Performance summary and comparison.

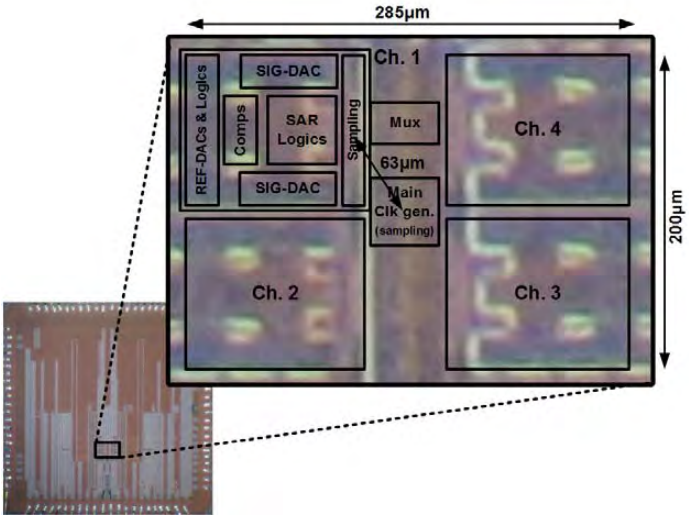


Figure 26.7.7: Die micrograph.

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Session 27 Overview: *Physical Sensors*

IMAGERS, MEMS, MEDICAL AND DISPLAYS SUBCOMMITTEE

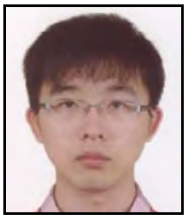
Session Chair: *Ralf Brederlow, Texas Instruments, Freising, Germany*

Session Co-Chair: *Michiel Pertijs, Delft University of Technology, Delft, The Netherlands*

This session presents recent achievements in the area of inertial, pressure, capacitance, magnetic, and temperature sensors. The first 3 papers are pushing power consumption, dynamic range, and drift of inertial sensors, enabling electronic stability control for new levels safety in the automotive sector and always-on navigation in mobile consumer devices. These presentations are followed by a fully integrated, small-form-factor tire pressure sensor. An innovative, energy-efficient read-out circuit for resonant sensors is followed by 2 presentations on energy- and area-efficient capacitance-to-digital converters. The session concludes with papers reporting a thermal-diffusivity-based temperature sensor for thermal monitoring, and a fluxgate-based magnetic-to-digital converter for contactless current sensing.

27.1 A 3-Axis Gyroscope for Electronic Stability Control with Continuous Self-Test **1:30 PM**
G. K. Balachandran, Robert Bosch, Palo Alto, CA

In Paper 27.1, Robert Bosch presents a 3-axis gyroscope for electronic stability control with continuous self-test. The system shows a 20dB higher dynamic range and strongly improved offset drift compared to state-of-the-art sensors.



27.2 A 1.2μg/√Hz-Resolution 0.4μg-Bias-Instability MEMS Silicon Oscillating Accelerometer with CMOS Readout Circuit **2:00 PM**
X. Wang, National University of Singapore, Singapore, Singapore

In Paper 27.2, the National University of Singapore and Nanjing University of Science and Technology demonstrate a MEMS accelerometer for inertial navigation applications with a record-low bias instability of 0.4μg. Its resolution of 1.2μg/√Hz is the highest reported to date.

27.3 A 3-Axis Open-Loop Gyroscope with Demodulation Phase Error Correction **2:30 PM**
C. D. Ezekwe, Robert Bosch, Palo Alto, CA

In Paper 27.3, Robert Bosch introduces a gyroscope architecture for consumer applications that reduces offset drift and consumes 3× less power than the state of the art.

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27.4 A 0.8mm³ ±0.68psi Single-Chip Wireless Pressure Sensor for TPMS Applications **2:45 PM**
M. B. Nagaraju, University of Washington, Seattle, WA

In Paper 27.4, the University of Washington and Avago Technologies describe a sensor principle enabling a sub-mm³ wireless pressure sensor for tire-pressure monitoring, more than 100× smaller than current systems.

27.5 A 30ppm <80nJ Ring-Down-Based Readout Circuit for Resonant Sensors **3:15 PM**
H. Jiang, Delft University of Technology, Delft, The Netherlands

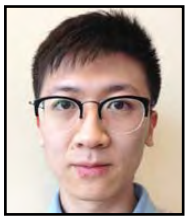
In Paper 27.5, TU Delft introduces a read-out circuit for resonant sensors capable of measuring resonance frequency and quality factor at 7.8× lower energy consumption than state-of-the-art systems.

27.6 A 0.7pF-to-10nF Fully Digital Capacitance-to-Digital Converter Using Iterative Delay-Chain Discharge **3:45 PM**
W. Jung, University of Michigan, Ann Arbor, MI

In Paper 27.6, the University of Michigan demonstrates a concept for capacitance-to-digital conversion that enables record-low energy efficiency and die size.

27.7 A 0.05mm² 1V Capacitance-to-Digital Converter Based on Period Modulation **4:15 PM**
Y. He, Delft University of Technology, Delft, The Netherlands

In Paper 27.7, TU Delft presents a capacitance-to-digital converter based on period modulation that employs several design innovations to reduce size and energy consumption.



27.8 A 4600µm² 1.5°C (3σ) 0.9kS/s Thermal-Diffusivity Temperature Sensor with VCO-Based Readout **4:30 PM**
R. Quan, Delft University of Technology, Delft, The Netherlands

In Paper 27.8, TU Delft introduces a highly digital thermal-diffusivity-based temperature sensor for use in SoC thermal monitoring. The sensor is the smallest for designs above 32nm.

27.9 A 200kS/s 13.5b Integrated-Fluxgate Differential-Magnetic-to-Digital Converter with an Oversampling Compensation Loop for Contactless Current Sensing **4:45 PM**
M. Kashmiri, Texas Instruments, Santa Clara, CA

In Paper 27.9, Texas Instruments describes an integrated fluxgate read-out sensor for contactless current sensing. It digitizes the magnetic field at 750× higher bandwidth than state-of-the-art systems.