26.6 A 5GS/s 150mW 10b SHA-Less Pipelined/SAR Hybrid ADC in 28nm CMOS

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The recent emergence of direct sampling in residential broadband satellite and cable receivers has spurred the need for low-power, high-speed (~5GS/s), mid-resolution (~10b) A/D converters. Recently, time-interleaved (TI) SARs have been a popular choice for low-power, medium-speed, mid-resolution ADCs [1-3]. As the conversion rate and resolution requirements increase, TI-SARs become less attractive in terms of power efficiency and complexity compared to TI-pipelined ADCs [4], where the critical SNR, THD, and TI matching are only required in the MDACs resolving the MSBs. In this paper we report a hybrid of TI-pipelined MDAC and TI-SAR, in which the former resolves the 2 MSB bits and the latter resolves the 8 lower bits. This hybrid architecture combines the advantages from each ADC type to achieve better power at 5GS/s. The front-end is implemented by time-interleaving two 2.5b MDAC slices, easing the timing-matching requirement and complexity. The MDAC stage also eases the timing-matching requirement among the TI-SARs by presenting an amplified-and-held signal to each SAR input. This allows taking advantage of a low-resolution SAR's simplicity and low power, for the last 8b. This work also proposes a SHA-less front-end to further minimize the ADC power. Two simple calibration techniques are introduced on-chip to enable the topology: (a) an over-range calibration (ORcal) loop to correct the sampling-time error between MDAC and sub-ADC in the SHA-less front-end, and (b) SAR reference calibration to align the SAR's full-scale to the MDAC's. Figure 26.6.1 shows the timing and functional block diagram of the 5GS/s hybrid SHA-less ADC. The RF buffer directly drives two TI-slices, each comprising a 2.5GS/s MDAC stage to resolve the 2.5 MSB bits, followed by 4-way interleaved 625MS/s SARs to resolve the lower 8b, for a combined 10b resolution (1b overlap), at 5GS/s.

The details of the front-end 2.5b MDAC, including the ORcal loop, are shown in Fig. 26.6.2. Removing the SHA and its noise, distortion, power, and area from the ADC budget is extremely attractive, but without a SHA, matching the voltages tracked and sampled by the MDAC and its sub-ADC becomes prohibitively challenging for multi-GHz input signals. The ORcal loop that we propose in this paper relaxes the matching requirements of sampling instant and bandwidth between the SHA-less MDAC and its sub-ADC, allowing a significant increase in the sampling speed of the ADC and its operational input BW. The ORcal loop works by adjusting the sampling instant of the sub-ADC with respect to the MDAC's. The quantization bits after the MDAC are observed to determine the *presence* and *sign* of any MDAC over-range voltage (if the residue exceeds $\pm V_{FS}/2$). Together, the input signal *slope* is determined. As shown in Fig. 26.6.2, four possible combinations of over-range sign and slope are identified, and based on the singular case, the ORcal loop determines whether the sub-ADC sampling instant needs to be advanced or delayed with respect to the MDAC's. The actuator (a simple capacitor-bank-based programmable delay in the sub-ADC's sampling clock path) is engaged until over-range disappears. Compared to previous works ([5], limited to 650MHz), based on trial-and-error, the loop proposed in this paper observes both over-range sign and input signal slope, and therefore the clock advance/delay decision is deterministic, resulting in fast and accurate convergence. As a result, the operational input BW exceeds the 2.5GHz Nyquist BW, as detailed later. By employing the ORcal, the sub-ADC's tracking network can be significantly scaled down, compared to the MDAC's, and the RF buffer power can be proportionally reduced. In the prototype, the 100fF sub-ADC sampling cap C_S is half of the MDAC's (C_R+C_F). The ORcal loop is engaged at start-up and can be left active in the background during normal operation. Its digital power is <5mW. The MDAC amplifier is similar as in [4].

Each 2.5GS/s 2.5b ping-pong MDAC is followed by a 4-way interleaved 625MS/s 8b SAR quantizer. Figure 26.6.3 shows a simplified single-ended diagram of the differential SAR. Each SAR ADC samples the input signal onto the top plate of the DAC capacitors. Binary-weighted sets of capacitors are sequentially controlled by a finite state machine (FSM). To avoid the use of power-hungry reference buffers, SAR ADCs use common external 1V supply and ground as positive and negative references (Vrp and Vrn), respectively. Use of the external supply also significantly improves DAC settling time, thus maximizing each SAR's throughput and in turn minimizing the amount of interleaving. The noise contribution from the reference is relaxed by the gain of the preceding 2.5b MDAC. The DAC settling is limited only by switch resistance and interconnect parasitic resistance to the supply. The SAR full-scale is determined by Vrp-Vrn, which in turn is attenuated by the capacitive attenuation factor β = Cdac / (Cdac + Cpar + Catt). The MDAC full-scale on the other hand is determined by a fixed supply voltage; thus a scheme to align the two full-scales is needed. The one-time calibration scheme shown in Fig. 26.6.1 illustrates how the SAR full-scale is aligned to that of the MDAC. A training signal whose level is equal to the MDAC full-scale is injected into the DAC input of the MDAC, and the Catt inside each SAR ADC is adjusted until the SAR ADC output reaches the target level equal to the SAR ADC's full-scale. Target level includes the SAR ADC's individual offset. After the full-scale of all SAR ADCs are aligned, SAR ADC's individual offset and gain mismatch among parallel SAR ADCs are calibrated out digitally. MDAC's full-scale is also referenced off the same external 1V supply. The alignment between the MDAC's and SAR ADC's full-scale is therefore locked across any supply voltage variation, eliminating the need to run the calibration in the background. Top-plate sampling is chosen over bottom-plate sampling, because it eliminates the β attenuation from the ADC input to the DAC output, thus minimizing the comparator noise when referred to the ADC input, and reducing its CK-Q delay.

The measurement results are shown in Figs. 26.6.4 and 26.6.5. Figure 26.6.4 shows the histogram of the SAR codes before and after the ORcal loop is engaged, for a 2.5GHz input signal. Under the hypothesis of no over-range and ideal MDAC settling, with 1b overlap between the two quantizers, the 8b SAR code max/min values should be bounded to +63/-64, and the code distribution should be approximately *uniform*, because the SAR digitizes the MDAC residue, whose transfer function is segmented. Before the ORcal loop is engaged, measured max and min SAR codes are +101 and -101, respectively, indicating presence of mild over-range in the MDAC residue, and the code distribution shows significant tails. The ORcal loop is demonstrated to reduce over-range, producing a much more uniform distribution, whose max/min tail codes are reduced to +74/-77, indicating a reduction in the MDAC output voltage swing by ~25% (therefore also improving the MDAC amplifier linearity). Figure 26.6.5 shows the ADC output's decimated spectrum, when the ADC, embedded in a heavily digital mass-production SoC, is clocked by a 5GHz, 250fs-jitter on-chip PLL [6]. For a 500MHz input at -0.5dBFS, the ADC achieves THD = -61.8dB and SNR = 57.1dB. For a high-frequency 2.35GHz input at -2dBFS, THD = -54.7dB. The TI spur ($f_S/2-f_{in}$) is < -70dBc. At this high input frequency, the on-chip PLL jitter dictates SNR/SNDR (46.8/46.1dB respectively). Measuring SNR with a small input and extrapolating to the same -2dBFS, the ADC SNR without PLL jitter is 55.8dB. No over-range is observed, up to 4.7GHz input (65% loading, limited by the instrument and production-PCB), proving the effectiveness of all schemes implemented, including SHA-less, ORcal, and MDAC/SAR reference calibration. Figure 26.6.6 shows a comparison of this work to state-of-the-art ADCs with similar conversion rate and resolution. The ADC consumes 150mW including power from reference and calibrations, and at 2.35GHz input achieves an FoM of 192.5fJ/conv and 95.8fJ/conv with and without PLL jitter, respectively. The corresponding Schreier FoMs are 148.1dB and 154.2dB, respectively. Figure 26.6.7 shows a die photo.

References:

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[6] B. Shen, *et al.*, "An 8.5 mW, 0.07 mm^2 ADPLL in 28nm CMOS with Sub-ps Resolution TDC and < 230 fs RMS Jitter", *Symp. VLSI Circuits*, pp C192-C193, 2013.

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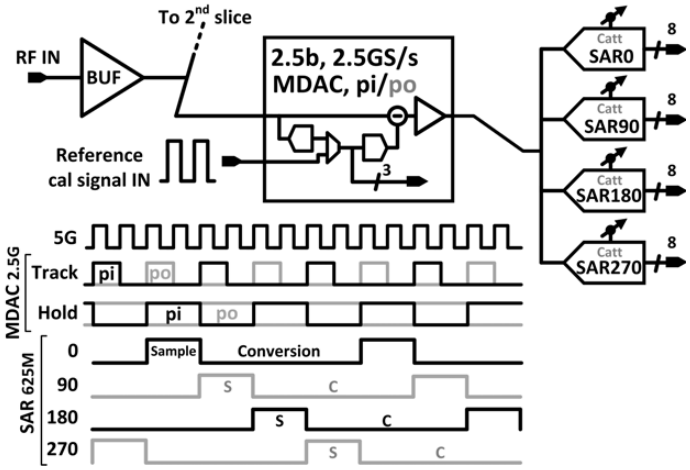

Figure 26.6.1: Functional diagram of the hybrid ADC (one slice, single-ended) and timing diagram (one slice).

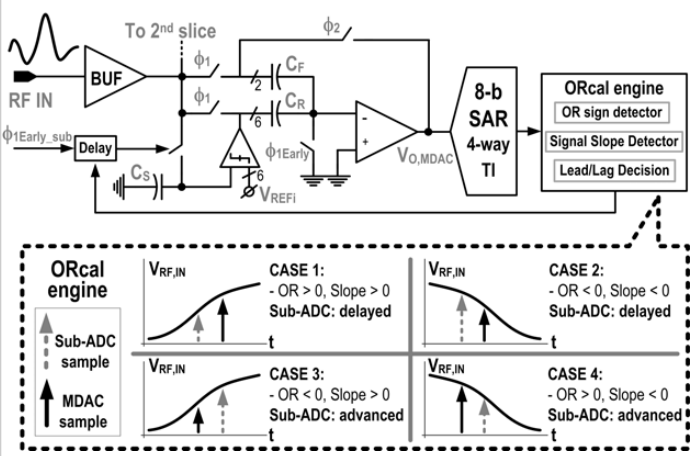

Figure 26.6.2: SHA-less ADC front-end conceptual block diagram (single-ended, one slice only, ping only) with on-chip ORcal loop.

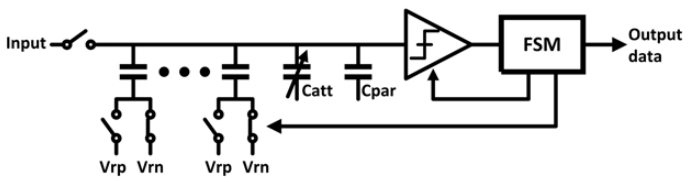

Figure 26.6.3: Simplified diagram of SAR ADC (differential half-circuit). Capacitor Catt is used to calibrate the SAR reference to match the MDAC's.

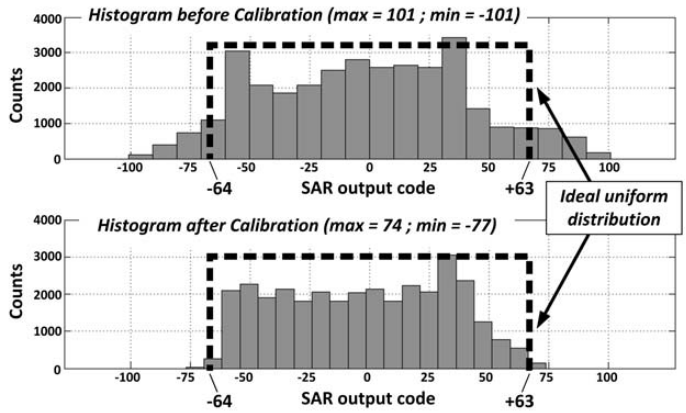

Figure 26.6.4: SAR output code before and after ORcal is engaged.

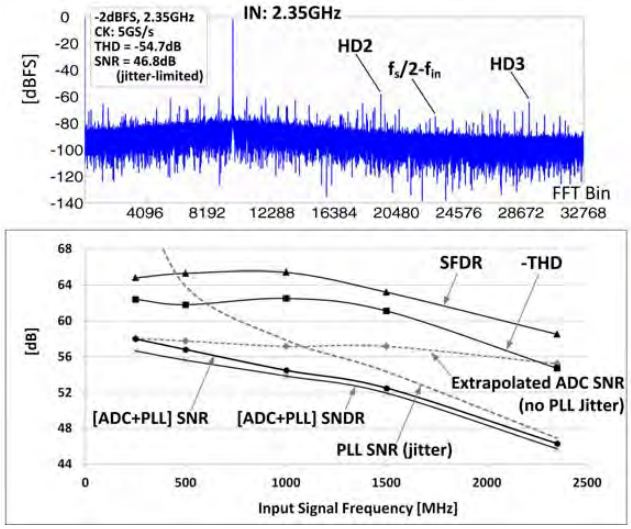

Figure 26.6.5: Decimated spectrum for a 2.35GHz input and ADC and PLL metrics Vs input signal frequency. Clock is 5GHz.

	This Work		[1] ISSCC 2013	[2] ISSCC 2014	[3] VLSI 2012
	With PLL Jitter	Without PLL Jitter			
Architecture	Pipe/SAR, TI		SAR, TI	SAR, TI	SAR, TI
f_S [GS/s]	5.0		3.6	1.6	2.8
Input [GHz]	2.35		1.7	0.48	1.4
THD [dB]	-54.7		-	-	-
SNR [dB]	46.8	55.8	-	-	-
SNDR [dB]	46.1	52.2	50	48	48.2
Power [mW]	150		795	93	44.6 (1)
Technology	28nm		65nm	40nm	65nm
Area [mm²]	0.45		7.4	0.83	0.18
FoM_{Walden} [fJ/c]	192.5	95.8	854.7	280	75.8 (1)
$FoM_{Schreier}$ [dB]	148.1	154.2	143.5	147	153.2 (1)

(1) Reference [3] excludes references and input buffer

Figure 26.6.6: Comparison with state-of-the-art multi-GS/s ADCs.

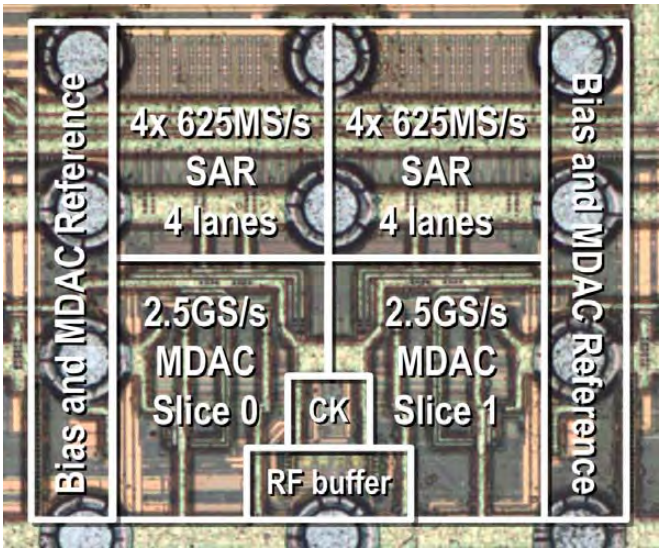

Figure 26.6.7: Die photo

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