26.4 A 21fJ/conv-step 9 ENOB 1.6GS/s 2× Time-Interleaved FATI SAR ADC with Background Offset and Timing-Skew Calibration in 45nm CMOS

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Recently reported high-speed ADCs have mostly taken advantage of time-interleaved (TI) architectures with low-power SAR ADCs for their sub-channels. However, given that the TI architecture needs to satisfy matching requirements between channels, the circuit complexity arising from the calibrations has often become a considerable burden. In order to reduce the number of channels in TI SAR ADCs, a flash-assisted TI (FATI) SAR structure [1] can be utilized to enhance the conversion speed of a sub-channel SAR ADC due to the multi-bit MSBs from a front-end flash ADC. In addition, because the codes from each SAR ADC embed the timing skew information of the corresponding channel, the structure can extract timing skew information in an efficient manner [2]. Despite these advantages of FATI SAR ADCs, as the required conversion rate increases, the power consumption of the front-end flash ADC becomes significant, which reduces the efficiency. In addition, if the target speed is higher than the frequency achievable by a single flash ADC, the FATI SAR ADC should be time-interleaved with multiple flash ADCs. The timing skew calibration scheme reported in [2] cannot be applied in this case. Considering these issues, this work introduces an advanced FATI SAR ADC with a folding-flash (F-flash) ADC that reduces the power burden placed upon a flash ADC. In addition, 2× time interleaving is applied in an effort to lower the conversion rate of the flash ADC (time-interleaved FATI SAR ADC). The offset and timing skew of each channel are calibrated in the background.

The architecture of the ADC and a timing diagram of a single channel are shown in Fig. 26.4.1. The entire ADC consists of odd and even channels of 10b FATI SAR ADCs, and each channel has one 4b F-flash ADC and six 10b SAR ADCs. Each SAR ADC works synchronously based on a clock to avoid unwanted reference fluctuations from the other channels while its CDAC settles. For the first two clocks (P_{samp}), the input (V_{IN}) is sampled, and during the following single clock period (P_{flash}), the F-flash ADC resolves 4b MSBs. Then, a single-channel SAR ADC determines 7b LSBs, including 1b redundancy for seven clock periods (P_{SAR}). In the final two clock cycles (P_{CAL}), offset or timing skew calibration is selectively performed; timing skew calibration is performed once after each of the eleven cycles of the offset calibrations.

Figure 26.4.2 shows the implementation of a single-channel 10b SAR ADC. For high-speed sampling, an 80fF sampling capacitor (C_{sample}) is used apart from the capacitor DAC, and bottom-plate sampling is used to ensure the linearity of the sampling. In order to eliminate the loading effect from the CDAC, the bottom plates of the CDAC capacitors are floated during the input sampling. A 1b sign code from the F-flash ADC is transferred to an MSB capacitor, 224C, whose value is determined for addition-only digital error correction [3]. 3b MSBs from the F-flash ADC are transferred to seven 32C unary capacitors in a 7b thermometer form. The rest of the CDAC is conventional, except that it has an additional 32C for redundancy between the F-flash and the SAR ADC.

A schematic of the F-flash ADC with the designated comparators is described in Fig. 26.4.3. The 4b F-flash ADC consists of a 1b sign detector (MSB) and seven comparators for the remaining 3b. Considering the speed penalty of conventional F-flash ADCs, which switch references after the determination of the sign bit, this work presents a modified comparator for the 3b ADC that has a dual-sampler with dual input-pairs to parallelize the reference-settling period with the sign-decision phase. During the sampling period of the F-flash ADC, each of the two sampling capacitor pairs samples the differential input (V_{INP} and V_{INN}). Subsequently, during the sign-decision period, references for both signs are readied by connecting one capacitor pair to the reference for sign<k> = 0 and connecting the other for sign<k> = 1 while the comparator is disabled with CLK_{flash}<k> = 0. When a comparator decision is required for 3b flash, only one latch path is enabled by the sign detector. By combining the reference settle time of the F-flash ADC with the sign-detection period, half the clock period of CLK_{MST} could be saved. In addition, the comparators used in the F-flash ADC are modified with regard to a conventional comparator for use with the FATI SAR ADCs. The comparator comprises six latches because the F-flash ADC needs to transfer its decision to six SAR ADCs. Each of the six latches in the comparator is each paired with one of the six SAR ADCs, which removes the registers for the MSB capacitors from each SAR ADC channel. Although the flash comparator clock (SEL_L or SEL_H) is disabled during the following SAR channel decision, the latch retains its output owing to MN_{hold}. As a result, 96 (8b × 12 channels) registers that would have been required for the 12 SAR ADCs are eliminated; accordingly, the related power consumption and propagation delay are removed.

Figure 26.4.4 depicts the principle of the timing skew calibration scheme, which uses a global time-reference clock (T_{REF}). T_{REF} is generated by dividing the external clock (CLK_{MST} (T_{CLK})) by 1/(1+N) [4] (N=12 channels), and it is distributed to every sub-channel, including the F-flash ADCs. For each timing skew calibration period (P_{cal}), a flash ADC and SAR ADC pair are selected in turn such that T_{REF} drives the same load. Note that the sampling clock (Q_{samp}<k>) of SAR ADC<k> has an additional sampling pulse within the P_{cal} phase for the timing skew calibration. Each sub-channel ADC, including the F-flash ADC, samples T_{REF} on C_{sample} during its own P_{cal} at its own delay-adjustable Q_{samp}<k>. The comparator in a sub-channel ADC then makes the direction of the timing skew between Q_{samp}<k> and T_{CLK} known; if Q_{samp}<k> lags T_{REF}, the comparator outputs "0", while in the opposite case, "1" is generated. From the result, the delayed external clock, CLK_D<k>, is adjusted and the timing skew between T_{REF} and Q_{samp}<k> is minimized. Note that the sampling edge of Q_{samp}<k> in P_{samp} is automatically calibrated using this skew calibration once the falling edge of the sampling pulse in P_{cal} has been calibrated. The skew calibration circuit is designed for a calibration range of 20.5ps with a step size of 160fs. The Q_{samp}<k> of the k-th channel is a combination of the master clock (CLK_{MST}) and its enable signals (En_{samp}<k>, En_{track}<k>). The sampling edge is determined by the CLK_{MST} to minimize the jitter and the spread of the timing skew. For the skew calibration, SAR ADCs utilize their own comparator, while each F-flash ADC incorporates a designated offset-calibrated comparator (not shown). The offsets of all comparators in this design are calibrated with a charge-pump-based offset calibration scheme, as in [1], during P_{cal}, when the channel is not involved in the timing skew calibration.

A prototype ADC implemented in 45nm CMOS occupies an active area of 0.36mm^2, including calibration circuits and the T_{REF} generator. At 1.6GS/s under a 1.1V supply, the total power consumption is 17.3mW. The analog power dissipated by the comparators, DACs and R-strings in the flash ADCs is 6.1mW, and the digital circuits consume 11.2mW. The measured SNDR and SFDR are 57.2dB and 68dB, respectively, at 1.6GS/s with a 17MHz input (Fig. 26.4.5). With a 790MHz input, the SNDR and SFDR are 56.1dB and 61.2dB, respectively. The SNDR stays above 56dB up to the Nyquist frequency. The background calibration of the offset and the timing skew improves the DNL and INL substantially to 0.42 LSB and 0.32 LSB from 19 LSB and 21 LSB, respectively. Figure 26.4.6 compares the prototype ADC with other state-of-the-art GHz ADCs. While the offset and skew errors are calibrated in the background, the prototype achieves an FoM of 21fJ/c-s at the Nyquist-input frequency.

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[1] B. Sung, *et al.*, "A 6 bit 2 GS/s Flash-Assisted Time-Interleaved (FATI) SAR ADC with Background Offset Calibration" *Proc. IEEE A-SSCC*, pp. 281-284, Nov. 2013.
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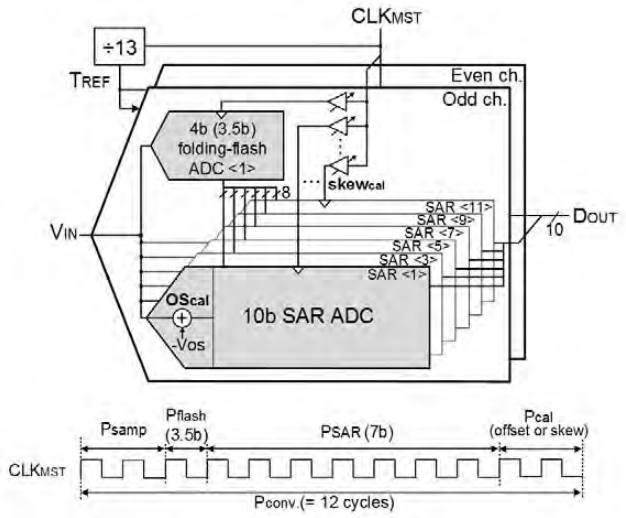

Figure 26.4.1: Block diagram of the 2× time-interleaved 10b FATI SAR ADC and timing diagram of a single-channel 10b SAR ADC.

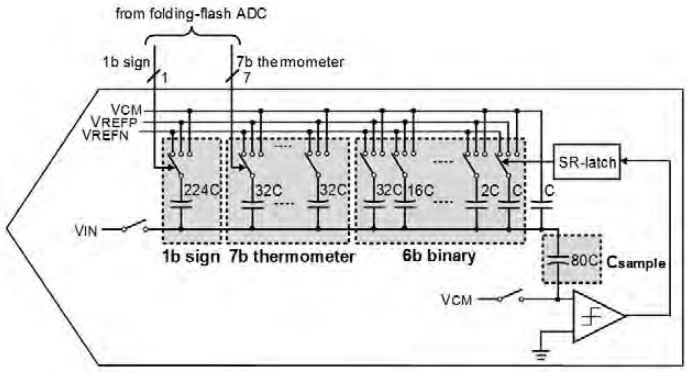

Figure 26.4.2: Single-channel 10b SAR ADC with a designated sampling capacitor (Csample).

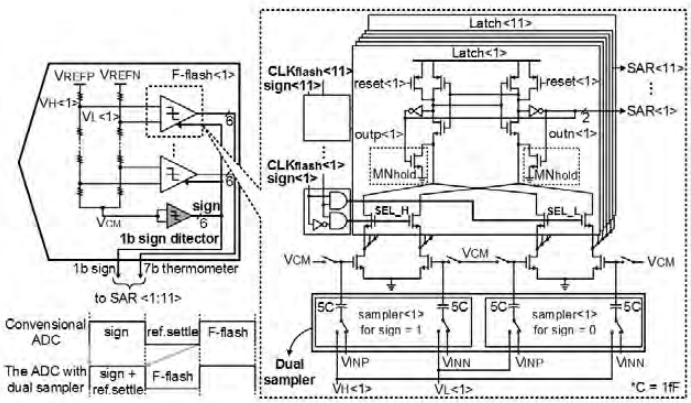

Figure 26.4.3: 4b folding-flash ADC with comparators that have dual input-pair/sampler and multiple latches.

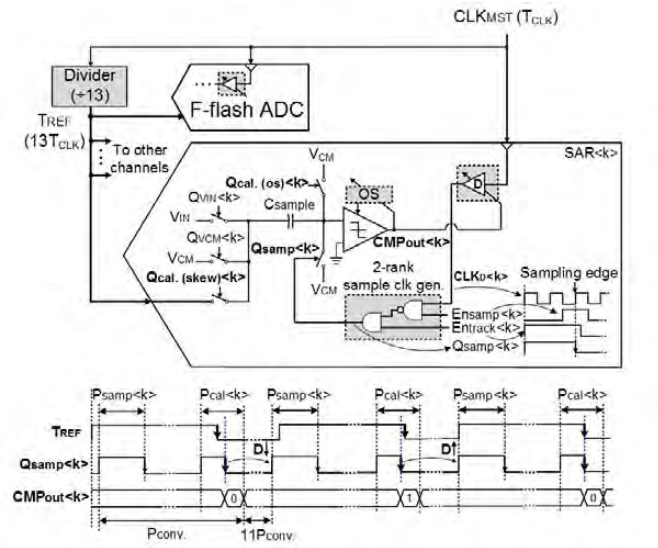

Figure 26.4.4: Timing skew calibration scheme.

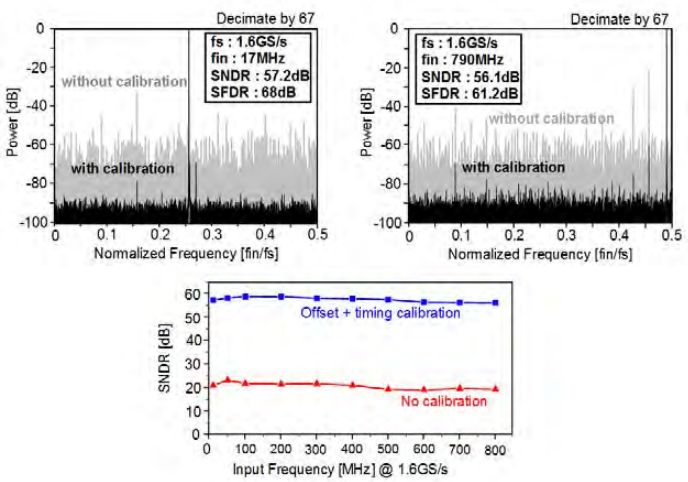

Figure 26.4.5: Measured dynamic performance.

10b ~GS/s ADC	ISSCC 14, N. Le Dortz	ISSCC 14, S. Lee	This work	CICC 12, Hashemi	JSSC 14, Hashemi
Architecture	TI-SAR	FATI-SAR	FATI-SAR	Pipeline	Pipeline
Technology [nm]	40	65	45	65	65
Resolution [bit]	9	10	10	10	9
Fs [MS/s]	1620	1000	1600	1000	1000
# of channles	12	8	12	-	-
Calibration type	g, os, time background	os, time fore. + back.	os, time background	gain foreground	offset foreground
Supply [V]	1.1	1.0	1.1	1.2	1
SNDR [dB] @Nyquist	48	51.4	**56.1**	52.7	48
Power [mW]	93	18.9	**17.3**	36	7.1
On-chip calib.	Yes	No	**Yes**	Yes	Yes
FoM[J/Conv.step] @ Nyquist	283f	62.3f	**21f**	70f	34f

*g : gain, os : offset

Figure 26.4.6: Performance summary and comparison.

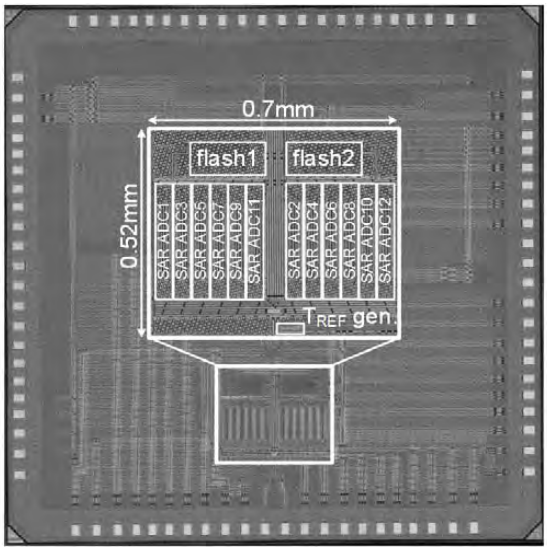

Figure 26.4.7: Die micrograph.

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