26.2 A 5.5fJ/conv-step 6.4MS/s 13b SAR ADC Utilizing a Redundancy-Facilitated Background Error-Detection-and-Correction Scheme

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Wireless standards, e.g., 802.15.4g, need high-resolution ADCs (>10b) with very low power and MS/s sampling rates. The SAR ADC is well known for its excellent power efficiency. However, its intrinsic accuracy (DAC matching) is limited up to 10 to 12b in modern CMOS technologies [1]. Scaling up the device dimensions can improve matching but it deteriorates power-efficiency and speed. Alternatively, calibrations [2-5] are introduced to correct errors (e.g., comparator offset and capacitor mismatch) and push the SNDR beyond 62dB. However, most of the calibrations [2-4] are implemented off-chip and the power for the calibration circuit is relatively high when implemented on-chip. Foreground calibration [4-5] is an alternative but is sensitive to environmental changes. We report a low-power fully automated on-chip background calibration that uses a redundancy-facilitated error-detection-and-correction scheme. Thanks to the low-power calibration, this ADC achieves an ENOB of 10.4b and a power efficiency of 5.5fJ/conv-step at 6.4MS/s.

The architecture of the ADC together with the conversion process is depicted in Fig. 26.2.1. It shows the S&H switches, the comparator, the SAR logic (15 cycles) and the feedback DAC. A total of 15 cycles is used to perform a 13b conversion, where the 7th and 11th cycles are redundant cycles similar to [6,7]. The 13b output is calculated from the 15b code by on-chip digital adders. The redundancy relaxes DAC settling requirements, enables the background calibration, and saves power using a two-mode comparator [6,7]: the comparator works in low-power mode (*mode1*) first and switches to high-precision mode (*mode2*) in the last 5 cycles, resulting in 2× energy reduction. A small total DAC capacitance (1.3pF) is achieved by using small unit capacitors. However, due to the small elements (0.3fF), the DAC matching is limited to <10b, which is not enough for a 13b ADC. Furthermore, a dynamic offset might also occur when the comparator switches from *mode1* to *mode2*. The automated background calibration can suppress both errors with negligible overhead in area or power.

The calibration logic is also shown in Fig. 26.2.1. It is only enabled for a limited set of SAR codes that are suitable for DAC or comparator calibration. This is detected by a *Sense&Force* block that enables an optional 16th comparison cycle to perform background calibration only for these specific codes. The results are stored in 6 calibration registers: 5 for the 5 calibrated MSBs of the DAC, and one for the comparator offset. Each register is preceded by an LPF to stabilize the calibration loop and to filter noise.

The goal of the comparator calibration is to equalize the offset for *mode1* and *mode2*, as it would otherwise result in a dynamic offset. To detect this offset difference, the optional 16th cycle repeats the same comparison as the 15th cycle. The DAC code remains unchanged, but the comparator switches from *mode2* to *mode1*. If the two results from these comparisons are different, it reveals the sign of the offset difference and thus the direction in which the comparator correction circuit needs to be tuned. Figure 26.2.2 depicts the analog correction method for comparator offset. The comparator switches from *mode1* to *mode2* during each conversion, causing an offset step (*offset2* – *offset1*). This is corrected by two programmable capacitors (C_a and C_b) that switch when the comparator changes mode, thus inducing a voltage step V_a-V_b that counteracts the offset step once the calibration is correctly settled. C_a and C_b use a binary-scaled bank of capacitors and allow an offset correction of up to ±63 LSB with 1 LSB steps. Note that the remaining offset error after calibration (within 1 LSB) is inherently compensated by the redundancy scheme.

Similarly, Fig. 26.2.2 also shows the analog correction method for the DAC mismatch: in parallel to a nominal capacitor, a set of binary-scaled capacitors can be programmed through a calibration control word (cal<k:0>). In such a way, the 5 MSBs of the ADC can be calibrated with steps of ¼ LSB. As the worst-case mismatch for the MSB is larger as compared to the lower ADC bits, the correction range is set to 15.5 LSB for the MSB, while smaller ranges are used for the lower bits. For DAC calibration, the principle is based on the detection of DNL errors, which indicates capacitor mismatch. Figure 26.2.2 (lower part) shows an example for the detection of the DNL error at the MSB. A similar picture could be drawn for the other bits of the DAC. This figure shows the INL with an exaggerated DNL error Δ due to MSB mismatch. Thanks to the redundancy, there is a convenient way to detect the sign of Δ, which is sufficient for the algorithm to tune Δ towards zero. The redundancy (i.e., 15 raw bits for a final 13b code) implies there are multiple 15b codes describing the same final 13b output. For instance, codes A and B (Fig. 26.2.2) resolve the same 13b output code and are thus equivalent. However, the bits inside code A and B are different, and hence the activated capacitors to generate these two codes are also different. If there is no capacitor mismatch, the sum of the activated capacitors in code A and B should be equal. On the other hand, if there is capacitor mismatch, the sum of the activated capacitors is not identical for codes A and B. This can be used as follows to perform a calibration: if code A is observed during a normal 15-cycle SAR conversion, a 16th cycle is added and an additional comparison is performed. Before the 16th cycle takes place, the internal code is updated to code B. In this way, the comparator result of the 16th cycle in comparison to the result in the 15th cycle determines whether the analog value of code A is larger or smaller than that of code B. With that information, the capacitors can be tuned to minimize Δ. Similar to the example given for the MSB, other detection codes can be used for the other bit transitions. All the detection codes are selected from the 2k-to-6k out of the 0-to-8k 13b code range, such that any sufficiently active analog signal at the ADC input obtains proper calibration. The calibration algorithm is activated for a limited set of SAR register values, thus reducing the occurrence to about 1% of all A/D conversions. This saves power while DAC mismatches and time-varying comparator offsets can still be calibrated properly. Thanks to the simple calibration algorithm and custom-designed dynamic logic, the active area of the digital calibration circuit is 0.0017mm^2, while the analog correction circuit is about 0.0009mm^2. Further, the direct error detection leads to a relatively short convergence time of <0.6s at 6.4MS/s according to Matlab simulations.

The SAR ADC is implemented in 40nm CMOS (Fig. 26.2.7) and occupies 0.0675mm^2. With calibration enabled, the ADC consumes 46µW from a 1.0V supply voltage at 6.4MS/s. Figures 26.2.3 and 26.2.4 show the INL/DNL and the spectrum with a near-Nyquist tone in three scenarios: without calibration, with comparator calibration and with both calibrations. The large initial DNL errors, caused by dynamic comparator offset, are effectively reduced when comparator calibration is enabled. The DAC calibration suppresses the INL errors due to DAC mismatch, as indicated in Fig. 26.2.3. The final INL is limited by sampling switch distortion. Still, the spurs due to comparator offset and DAC mismatch are suppressed by 20dB (Fig. 26.2.4). Therefore, the SNDR and SFDR are enhanced to 64.1dB and 81.9dB at Nyquist, respectively, achieving a 5.5fJ/conv-step FoM. Figure 26.2.5 shows the dynamic performance with calibration enabled and the scaling of the power consumption (133nW leakage level) with sampling rate. The measurement results are summarized in Fig. 26.2.6. This ADC achieves a lower FoM than for state-of-the-art ADCs reported in Fig. 26.2.6, while also integrating an on-chip background calibration technique for comparator offset and DAC mismatch.

References:

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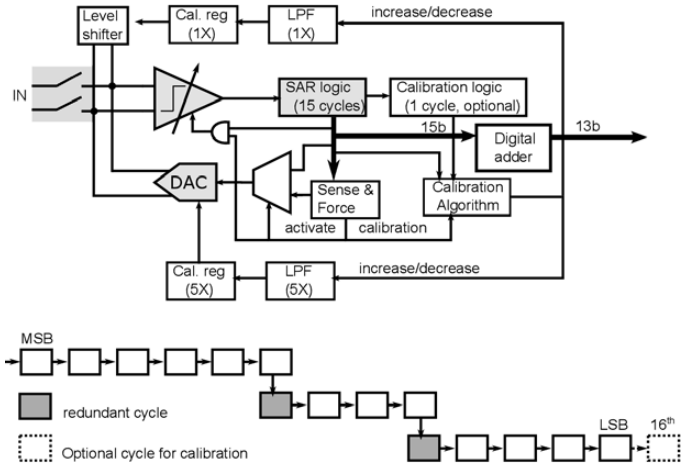

Figure 26.2.1: ADC architecture and 13b conversion scheme with 2 redundant cycles and an optional calibration cycle.

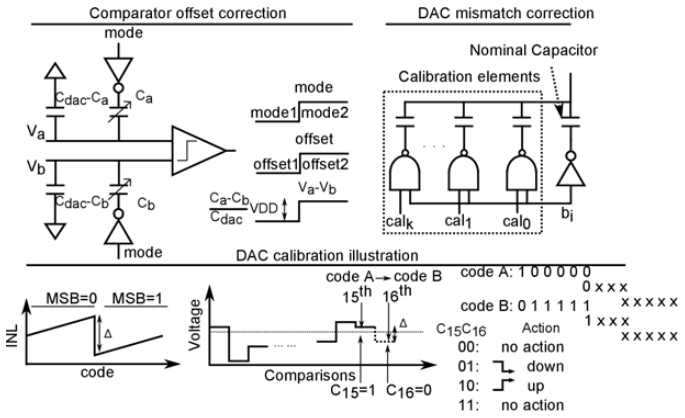

Figure 26.2.2: Analog correction scheme for the comparator and DAC, as well as an illustration of the DAC calibration.

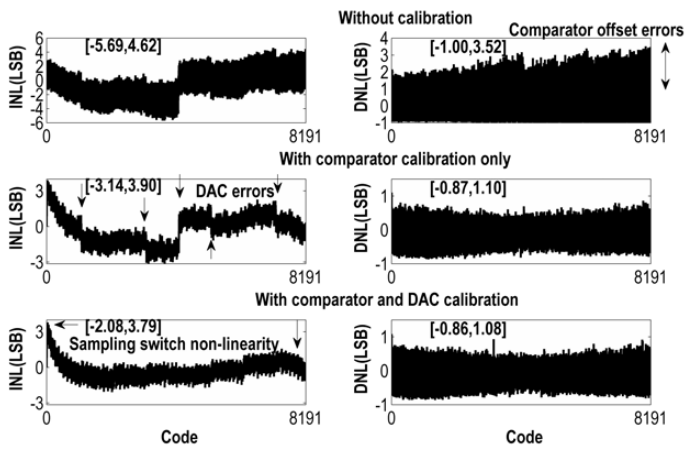

Figure 26.2.3: INL/DNL in three scenarios: without calibration, with comparator calibration only and with both calibrations.

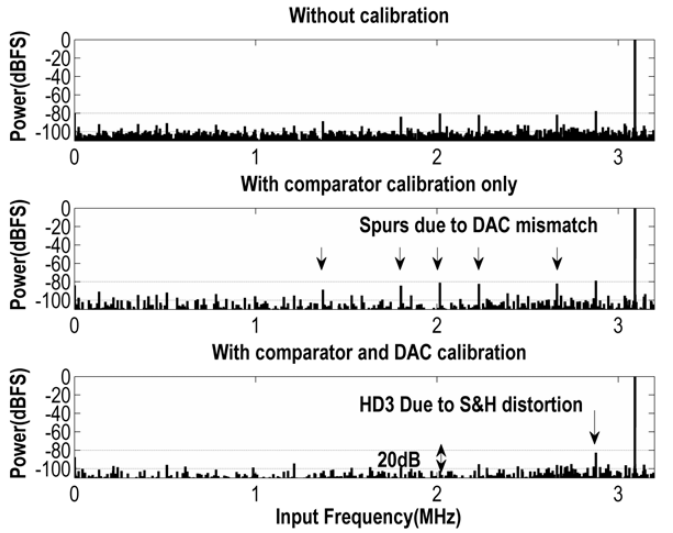

Figure 26.2.4: Spectrum with a near-Nyquist tone in three scenarios: without calibration, with comparator calibration only and with both calibrations.

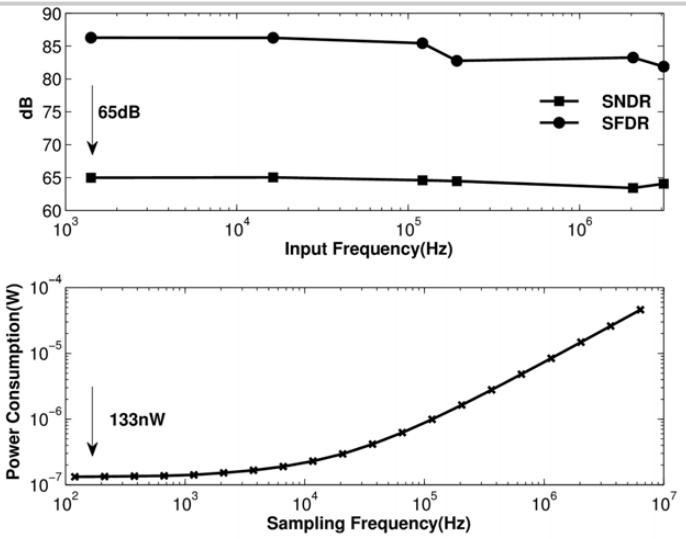

Figure 26.2.5: Dynamic performance at 6.4MS/s and power consumption versus sampling frequency.

	[2]		[3]	[4]	[5]	This work
Architecture	SAR		Pipelined SAR	Pipelined SAR TI	Pipelined SAR TI	SAR
Technology (nm)	130		40	28	28	40
Area (mm^2)	0.059		0.042	0.35	0.1369	0.0675
Resolution (bit)	12		12	14	14	13
Supply voltage (V)	1.2		1.1	0.9	1.0	1.0
Reference Voltage (V)	1.2		1.0	0.9	1.8	1.0
Sample rate (MS/s)	22.5	45	160	200	80	6.4
Power (uW)	2790	2820	4960	2300	1500	46
INL (LSB)	-	-	-	2	-	3.79
DNL (LSB)	-	-	-	2	-	1.08
Nyquist SNDR (dB)	70.11	67.09	65.3	65	66	64.1
Nyquist SFDR (dB)	90.31	84.71	85	-	74	81.9
FOMW_Nyquist (fJ/conv.step)	50.8	36.3	20.7	7.9	11.5	5.5
Calibration	Off-chip		Off-chip	Off-chip	On-chip	On-chip
Cal. Circuit Area (mm^2)	0.01*		Not included	Not included	Included	0.0026
Cal. Circuit Power(uW)	200*		100**	Not included	Included	Included

*Estimated by SPICE
** Estimated power by software

Figure 26.2.6: Performance summary and comparison with state of the art.

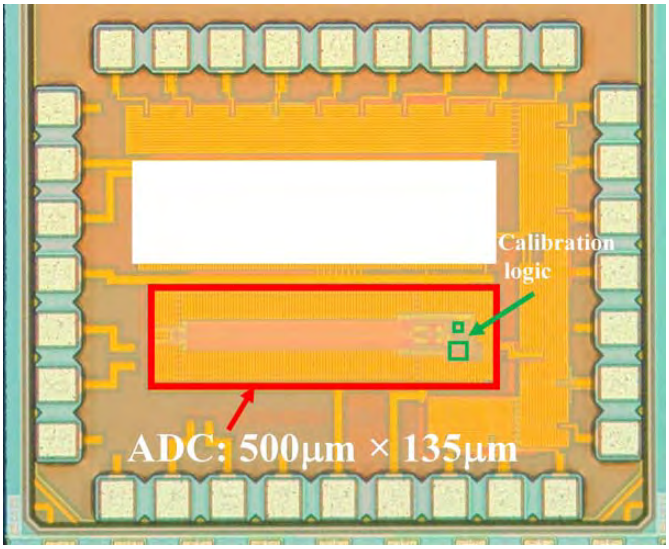

Figure 26.2.7: Chip photo.

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