25.9 A ±3ppm 1.1mW FBAR Frequency Reference with 750MHz Output and 750mV Supply

Kannan A. Sankaragomathi[1], Jabeom Koo[1], Richard Ruby[2], Brian P. Otis[1]

[1]University of Washington, Seattle, WA, [2]Avago Technologies, San Jose, CA

Multiple emerging wireless applications (body-worn devices and IoT, for example) will demand previously impossible thin-film form factors and low system cost. One key enabling technology for this paradigm is a new class of radios that offer cost/size approaching RFID while still maintaining peer-to-peer connectivity like more complex radios. These radios need to be cheap and thin, which means they should be fabricated using wafer-scale semiconductor processing. The existing paradigm (quartz crystals used as a frequency reference in radios) is a huge bottleneck in reducing cost and size of these devices. MEMS frequency references have replaced quartz crystals in some applications [1-3]. For example, [1] reports a MEMS reference with 0.5ppm stability but the power consumption (~100mW) and supply voltage (1.8V) are not suitable for low-voltage/low-power radios. [2] reports a 32kHz, 3ppm reference for mobile time-keeping applications, but is unsuitable for radio frequency synthesis due to its low output frequency. In this paper, we report a thin-Film Bulk-Acoustic-Resonator (FBAR) frequency reference suitable for low-voltage/low-power radio applications. The reported FBAR reference achieves a stability of +/- 3ppm from 0 to 90C. We achieve this by using an electronic temperature compensation scheme to improve the intrinsic +/-50ppm stability of an FBAR oscillator down to +/- 3ppm (Fig. 25.9.1). The core of the temperature compensation scheme is a temperature sensor that achieves a 1.75mK resolution at a 100mS sampling time.

Figure 25.9.1 shows the block diagram of the FBAR frequency reference. Transistors MP1 and MN1 form a Pierce oscillator. The oscillator in this work operates at 750MHz, but the frequency can be changed to any frequency (>500MHz & <10GHz) at design time by using an appropriate FBAR. The oscillator operates from a 650mV regulated supply voltage generated using a low voltage bandgap reference and an LDO. A 6b thermometric MIM cap array is used to stabilize the oscillator frequency to the targeted value. The cap array has a tuning range of 300ppm; sufficient to correct the frequency for temperature and process variations. The raw tuning resolution of the cap array is ~ 5ppm, and a 2nd-order $\Delta\Sigma$ modulator runs from a divided-by-4 clock and dithers the cap array, improving the resolution to <5ppb. A thermometric cap array and top-bit-dithering (dithering is dynamically pointed at the last bit in the array) provide a monotonic frequency tuning without any abrupt frequency jumps. A 0.75V digital temperature sensor generates a 19b word proportional to absolute temperature. A calibrated polynomial computation engine (supports up to a 4th-order polynomial) converts the temperature sensor output to an appropriate frequency control word to stabilize the oscillator. A one-time calibration is needed to estimate the coefficients of the polynomial generator. The temperature sensor that forms the core of the temperature compensation scheme is described in detail below.

We introduce a new temperature sensor architecture that is motivated by the fact that the FBAR oscillator provides a very-high-quality (low-noise, low-drift) time reference. The 750MHz oscillator output is divided to lower frequencies to run the $\Delta\Sigma$ modulator and the digital computation engine. These existing divided clocks give us a very precise time domain DAC which is exploited to achieve a low-voltage operation. Figure 25.9.2 explains the basic principle of the temperature-sensing scheme. A Wheatstone bridge is constructed using two types of resistors R_P (N-well) and R_M (p-poly). R_P has a positive temperature coefficient i.e $R_P = R_{P0}(1 + \alpha T)$ while R_M has a negative temperature coefficient i.e. $R_M = R_{M0}(1 - \beta T)$. R_M is split into a fixed component $R_{M,fixed}$ and a variable component $R_{M,var}$ whose average value is controlled by the duty cycle of CLK_C. A feedback loop using a zoom-ADC adjusts the average duty cycle, *d* of CLK_C to ensure a balanced bridge. The duty cycle under this condition is given by

$$d \cong \frac{R_{P0}}{R_{M,var\,0}}\,(1+(\alpha+\beta)T) - \frac{R_{M,fixed0}}{R_{M,var0}}$$

This mechanism encodes the temperature in the time domain enabling us to fully exploit the available accurate time reference and to achieve a low voltage operation. A 10b digital-to-duty-cycle converter (DDC) uses divided clocks from the clean oscillator to generate CLK_C with a 200kHz frequency and a variable duty cycle (see Fig. 25.9.3). The DDC, together with an integrator and comparator forms a zoom ADC.

The zoom ADC operates in two phases: a SAR phase and a $\Delta\Sigma$ phase. In the SAR phase the feedback loop digitizes *d* to a 7b coarse value and bounds its value between two levels: d_{ref1} and d_{ref2}. Then, the loop is rearranged to form a first-order $\Delta\Sigma$ loop that dithers the DDC control between d_{ref1} and d_{ref2}, obtaining a finer 19b digital estimate of *d*. After offset and scaling, *d* provides the required ambient temperature measurement. The integrator used in the zoom ADC is shown in Fig. 25.9.3 [5]. The integrator uses chopping to remove 1/f noise. The zoom operation relaxes the swing required across the integrator to within 100mV, leaving ~600mV headroom for the 4-transistor stack. All biases use bandgap-referenced feedback loops to ensure 150mV V_{ds} for all transistors across process and temperature.

The FBAR frequency reference was fabricated in a 65nm TSMC process. Figure 25.9.4 (top) shows the temperature stability of the compensated FBAR reference measured from 3 different chips. The oscillator achieves a stability of +/- 3ppm across 0 to 90C. Figure 25.9.4 (bottom) shows the phase noise of the oscillator with and without the temperature compensation turned on. There is no significant phase noise degradation due to the temperature sensor or the $\Delta\Sigma$ modulator. Spurs present in the spectrum are due to on-chip 24kHz logic and a 32× serializer running at 738kHz. In this chip 24kHz was used due to legacy reasons. In future iterations the logic clock frequency can be reduced to 10Hz pushing the spurs below the noise floor. The temperature-compensated frequency reference achieves an Allan deviation of 8ppb at a 100mS integration time which is competitive with current MEMS frequency references. The reported FBAR frequency reference consumes a total power of 1.1mW from a 0.75V supply. The oscillator consumes 450µW, the temperature sensor consumes 15µW, and the rest is consumed by the buffers, dividers, $\Delta\Sigma$ modulator and the digital polynomial generator. Figure 25.9.5 presents measured results for the temperature sensor from a sample of 3 chips. After a 4-point calibration, the temperature sensor achieves an accuracy of 0.2°C, sufficient to achieve a frequency stability of ±3ppm. The temperature sensor achieves a resolution of 1.75mK with a sampling time of 100ms. This corresponds to a resolution FOM of 4.6pJK^2. (excluding power of the shaded digital blocks in Fig. 25.9.2 for fair comparison with previous works). This is a 3× improvement over the state-of-the-art sub-1V temperature sensor presented in [4] and is comparable to the state-of-the-art high-voltage temperature sensor described in [6]. Figure 25.9.5 (top) shows the frequency of the oscillator over a span of 11 hours. Figure 25.9.6 compares the reported temperature sensor to state-of-the-art temperature sensors, and also compares the FBAR frequency reference to other MEMS and quartz references. In contrast to previously reported MEMS references, this work presents an RF frequency reference with sufficient stability (+/-3ppm) and power (1.1mW) suitable for quartz-free standards-based wireless transceivers.

References:

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[2] Asl et. al, "A 1.55x0.85mm^2 3ppm 1.0µA 32.768kHz MEMS-Based Oscillator", *ISSCC Dig. Tech. Papers,* pp. 226-227, Feb. 2014.

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[4] Souri et. al, "A 0.85V 600nW all CMOS Temperature Sensor with an Inaccuracy of +/- 0.4C from -40 to 125C", *ISSCC Dig. Tech. Papers,* pp. 222-223, Feb. 2014.

[5] Shahmohammadi et. al, "A resistor based temperature sensor for MEMS frequency references," *European Solid-State Circuits Conference, (ESSCIRC)*, pp. 225-228, Sept. 2013.

[6] Heidary et. al, "A BJT-Based CMOS Temperature Sensor with a 3.6 pJK^2 Resolution FOM", *ISSCC Dig. Tech. Papers*, pp. 224-225, Feb. 2014.

[7] TXC datasheet available online 'www.txccrystal.com/images/pdf/8p.pdf'.

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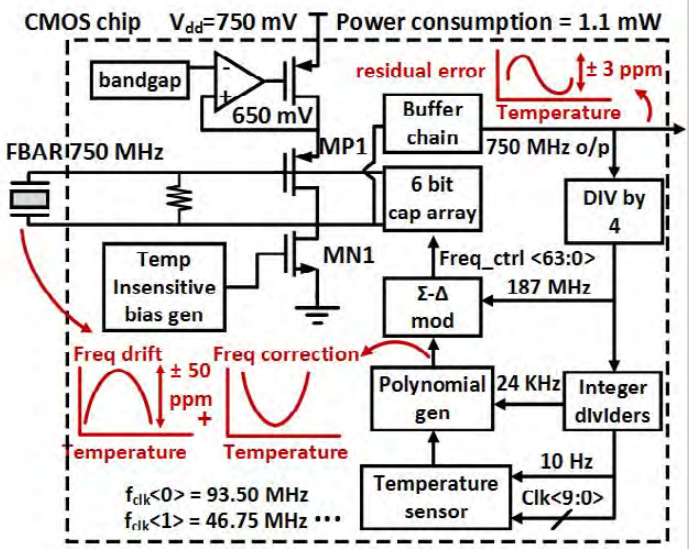

Figure 25.9.1: Architecture of the FBAR frequency reference.

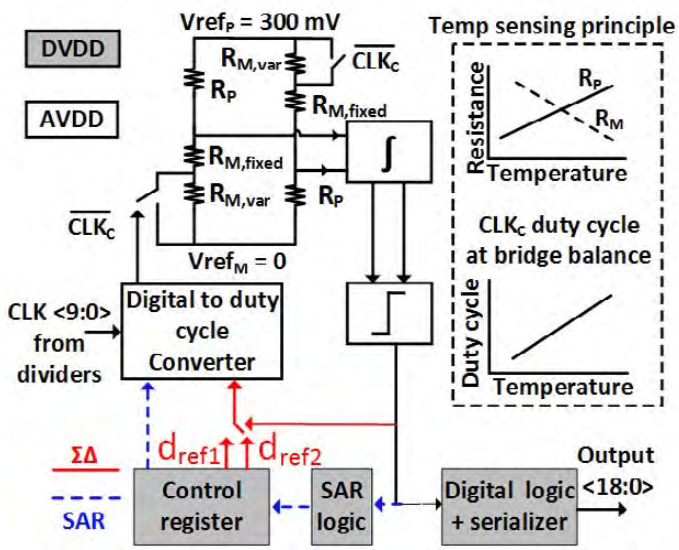

Figure 25.9.2: Principle and architecture of the temperature sensor.

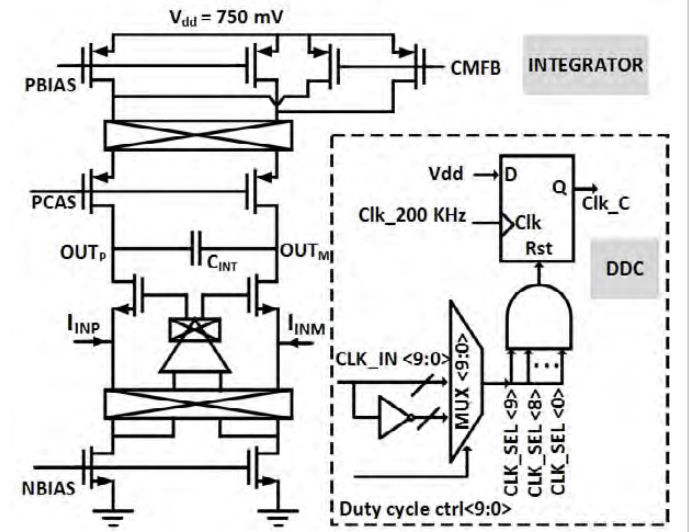

Figure 25.9.3: Integrator and the digital to duty cycle converter(box) used in the Zoom ADC.

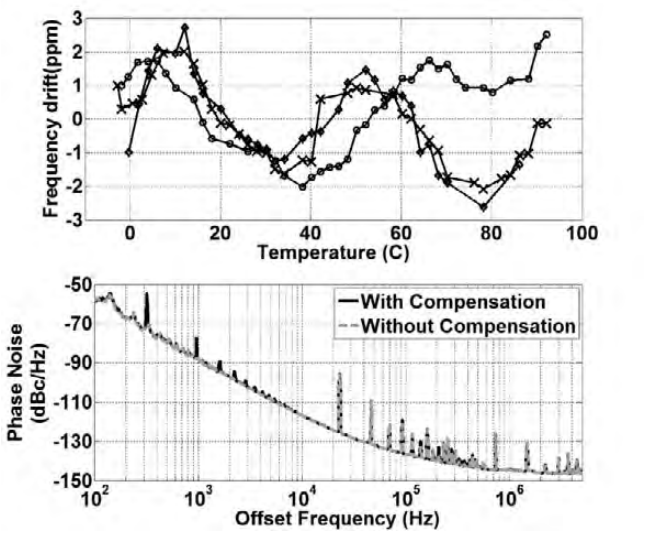

Figure 25.9.4: Measured frequency drift across temperature (3 chips) and phase noise of the FBAR reference.

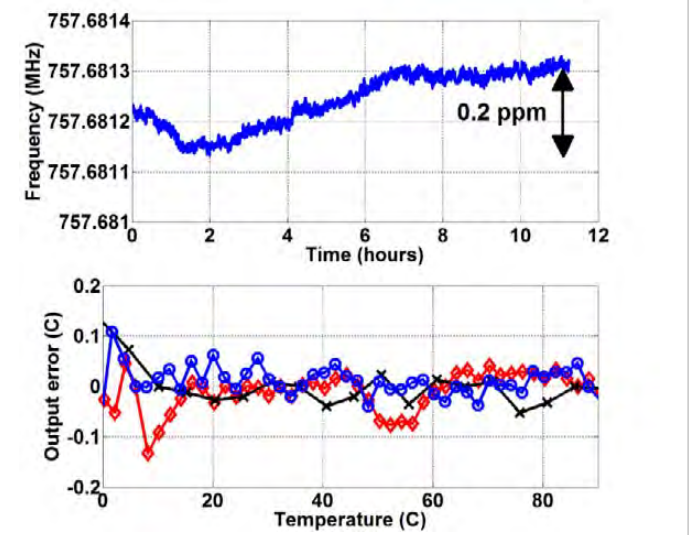

Figure 25.9.5: Measured frequency of the FBAR reference for 11 hours and measured error of temperature sensor (3 chips).

Frequency reference performance comparison				
Performance metric	**[2]**	**[1]**	**[7]**	**This Work**
Frequency	32 KHz	1-330MHz	26 MHz	**750 MHz**
Supply Voltage (V)	1.2	3.3	1.8	**0.75**
Power consumption (mW)	0.001	108	3.6	**1.1**
Size (mm x mm)	1.55 x 0.85	2.02 x 1.89	1.6 x 1.2	**1.4 x 0.8 (CMOS) + 0.5 x 0.5 (FBAR)**
Stability (ppm)	3	+/-0.2	+/- 2	**+/- 3**
Temp. range (C)	-40 to 85	-40 to 85	-40 to 85	**0 to 90**
Phase noise @ 1MHz (normalized to 750 MHz)	NA	-124	NA	**-145**
Allan dev @0.1s (ppb)	NA	4	NA	**8**
Technology	0.18 um	0.18 um	NA	**65nm**
Temperature sensor performance comparison				
Performance metric	**[4]**	**[6]**	**[5]**	**This Work**
Supply voltage (V)	0.85	2.9	1.8	**0.75**
Power consumption(uW)	0.6	159	36	**15**
Temp. range (C)	-40 to 125	-45 to 130	-40 to 85	**0 to 90**
Resolution (mK)	63	3	6	**1.75**
Integration time (ms)	(6)	(2.2)	(100)	**(100)**
Resolution FOM (pJK^2)	14.1	3.6	130	**4.6**
No. of trims	1	1	3	**4**
Accuracy (C)	0.4	0.15	0.15	**0.2**

Figure 25.9.6: Performance summary and comparison table.

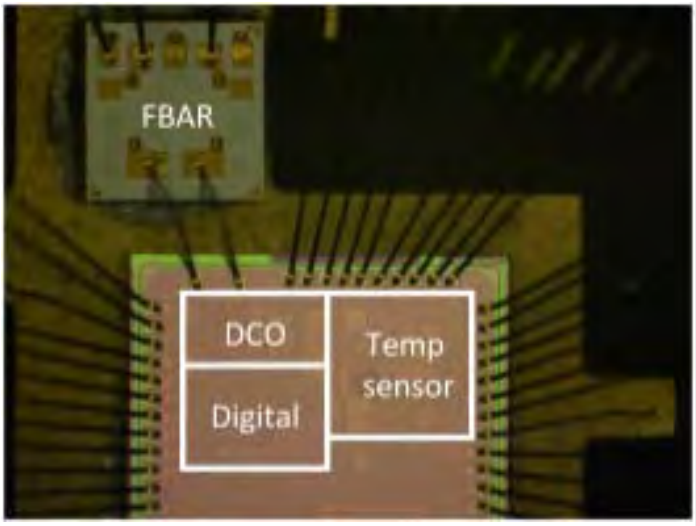

Figure 25.9.7: Assembly of CMOS chip with FBAR die.

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Session 26 Overview: *Nyquist-Rate Converters*

DATA CONVERTERS SUBCOMMITTEE

Session Chair: *Hae-Seung Lee, Massachusetts Institute of Technology, Cambridge, MA*

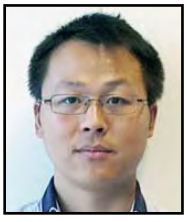
Session Co-Chair: *Seng-Pan U, University of Macau, Macau, China*

Innovative circuit and architecture techniques are the driving force in improving the efficiency of state-of-the-art Nyquist-rate data converters. In this session, creative approaches including new amplifier topologies, a wide variety of calibration schemes to remove errors resulting from finite gain, insufficient settling, and timing skew, as well as energy efficient data conversion techniques are presented.

26.1 A 1mW 71.5dB SNDR 50MS/s 13b Fully Differential Ring-Amplifier-Based SAR-Assisted Pipeline ADC **1:30 PM**

Y. Lim, University of Michigan, Ann Arbor, MI and Samsung Electronics, Yongin, Korea

In Paper 26.1, the University of Michigan present a SAR-assisted 2-stage pipeline ADC that employs a fully differential ring amplifier. Built in a 65nm technology, the converter achieves 71.5dB SNDR and 6.9fJ/conversion-step FoM at 50MS/s from a 1.2V supply.



26.2 A 5.5fJ/conv-step 6.4MS/s 13b SAR ADC Utilizing a Redundancy-Facilitated Background Error-Detection-and-Correction Scheme **2:00 PM**

M. Ding, Holst Centre / imec, Eindhoven, The Netherlands

In Paper 26.2, Holst Centre/imec and TU Eindhoven present background calibration for capacitor mismatch in a SAR ADC. The capacitor mismatch is measured by switching the DAC code to its redundant counterpart in an optional extra clock cycle. Utilizing a 2-mode comparator for better power efficiency, the converter achieves 5.5fJ/conversion-step FoM at 6.4MS/s.

26.3 An 800MS/s 10b/13b Receiver for 10GBASE-T Ethernet in 28nm CMOS **2:30 PM**

D. Vecchi, Broadcom, Bunnik, The Netherlands

In Paper 26.3, Broadcom presents a resolution-configurable pipeline ADC for a 10GBASE-T receiver. The resolution can be reduced to 10b for short cable lengths to achieve lower power consumption in the receiver. Aided by residue amplifier gain calibration, a peak ENOB of 9.54 is achieved at 800MS/s.

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26.4 A 21fJ/conv-step 9 ENOB 1.6GS/s 2× Time-Interleaved FATI SAR ADC with Background Offset and Timing-Skew Calibration in 45nm CMOS **3:15 PM**

B-R-S. Sung, KAIST, Daejeon, Korea

In Paper 26.4, KAIST and Samsung introduce a 1.6GS/s 10b Flash-assisted 2× time-interleaved SAR ADC where each channel consists of a 4b folding-Flash and 6 SAR ADCs. With background offset and timing skew calibration, the ADC achieves 9 ENOB with energy efficiency of 21fJ/conversion-step.

26.5 A 5.5mW 6b 5GS/s 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS **3:45 PM**

C-H. Chan, University of Macau, Macao, China

In Paper 26.5, the University of Macau presents a 6b 5GS/s converter that interleaves 3b/cycle SAR ADCs with simplified hardware and operation phases, leading to 39fJ/conversion-step FoM without timing skew calibration. A boundary-detection-code-overriding scheme improves the ADC error rate due to metastability.

26.6 A 5GS/s 150mW 10b SHA-Less Pipelined/SAR Hybrid ADC in 28nm CMOS **4:15 PM**

M. Brandolini, Broadcom, Irvine, CA

In Paper 26.6, Broadcom demonstrates a 28nm CMOS 10b pipelined/SAR hybrid ADC operating at 5GS/s. The ADC combines a 2.5b 2-way interleaved MDAC and 8b 8-way interleaved SAR ADCs with over-range calibration loops to allow SHA-less operation. The ADC consumes 150mW power including input and reference buffers.

26.7 A 2.6b/cycle-Architecture-Based 10b 1.7GS/s 15.4mW 4×-Time-Interleaved SAR ADC with a Multistep Hardware-Retirement Technique **4:45 PM**

H-K. Hong, KAIST, Daejeon, Korea

In Paper 26.7, KAIST and Samsung introduce a 2.6b/cycle, 4× time-interleaved SAR ADC with a multi-step reconfiguration technique that disables hardware blocks after respective bit decisions are made, resulting in an energy efficiency of 30.4fJ/conversion-stop at 1.7GS/s in 45nm CMOS.