25.8 A 2.4GHz VCO with FOM of 190dBc/Hz at 10kHz-to-2MHz Offset Frequencies in 0.13µm CMOS Using an ISF Manipulation Technique

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For the last few decades, phase-noise (PN) improvement of VCOs has been an intriguing problem and remains as one of the challenges in transceiver design. PN in CMOS VCOs, especially close-in PN, greatly suffers from flicker noise. The flicker noise can even degrade the PN at higher offset frequencies (~1MHz). The close-in PN is important in many communication applications. For instance, IEEE 802.11a/b/g requires a very low PN at 10kHz offset frequency [1] and the PN performance at 100kHz is critical in cellular and Wi-Fi MIMO applications. In addition to the PN performance, oscillators with lower power consumption and smaller area are always on demand.

In conventional cross-coupled VCOs, the tail transistor has a large contribution to the PN, especially at close-in offset frequencies [2]. Many efforts have been made to suppress the tail noise. In [2], a trap is placed at the drain of the tail transistor to block the tail noise around the second harmonic of the oscillation frequency. This requires an extra inductor and also does not considerably decrease the contribution of the flicker noise. In the Class-D VCO in [3], though the tail transistor is removed, the PN is greatly affected by the flicker noise since the main transistor flicker noise is directly injected to the tank. Moreover, the output spur level is degraded. To the best of our knowledge, no specific method to decrease the tail flicker noise is presented in the literature.

We use the Impulse Sensitivity Function (ISF) concept [4] to manipulate a cross-coupled oscillator and design a 2.4GHz VCO with a PN of -88.7dBc/Hz and -128.4dBc/Hz at 10kHz and 1MHz offset frequencies respectively, with no more power consumption and area overhead. The proposed structure almost completely eliminates flicker noise contribution to the PN above 10kHz offset frequencies. To explain the proposed oscillator, let us consider the tail ISF (Γ_{tail}) waveform of a conventional cross-coupled oscillator in Fig. 25.8.1 (In this paper the output voltage is considered as Acos(φ) where $\varphi = \omega_0 t$). ISF of a noise source shows the sensitivity of output phase variation to the noise injection time in a period. Since the tail noise is stationary, its noise modulation function (NMF, α) is almost equal to 1. Hence, the effective tail ISF is almost the same as its ISF, [4] ($\Gamma_{tail,eff} = \Gamma_{tail} \times \alpha_{tail} \simeq \Gamma_{tail}$). In order to improve PN, we need to lower the $\Gamma_{tail,eff}$ by manipulating both α_{tail} and Γ_{tail}. In what follows we present a technique to lower both of these parameters.

To minimize $\Gamma_{tail,eff}$, we make α_{tail} almost zero when the corresponding Γ_{tail} is large. This can be achieved by turning off the tail transistor at the peaks of Γ_{tail}. Considering the Γ_{tail} waveform, switching off should be done at least twice in each period. This is challenging as it requires extraction of second harmonic with proper phase shift which is not very efficient and reliable at RF frequencies. A better solution is to use two split current sources at the tail and switch them separately with a frequency of f_0 (oscillation frequency). We can also separate the two transistors, to individually turn on and off each branch. Schematic of the new cross-coupled oscillator with a cyclo-stationary tail is shown in Fig. 25.8.2. Network, RC_1, connects the gates of driver transistors to the output of the oscillator. Based on the oscillation frequency and the values of R and C_1, one can control the switching time to minimize α_{tail}.

Next, we make Γ_{tail} smaller. As shown in Fig. 25.8.1, the tail noise has two different paths to flow. The first is through M_1 (M_2) to the output, which results in PN and the second path is through M_3 to ground. The tail noise mostly tends to flow in the first path since the impedance seen from source of M_1 (M_2) is much smaller than the drain of M_3. To prevent the tail noise from flowing to the output, we create a low impedance path to the ground at the tail. This means the tail noise can directly be diverted to ground. Basically with a fixed noise power at the tail, a smaller portion of it flows to the output, which means the output phase is less sensitive to injection of a specific amount of noise power at the tail. This means the Γ_{tail} amplitude becomes smaller. As shown in Fig. 25.8.2, we can create a low impedance path to ground at the tail by replacing the tail transistors with PMOS devices. Γ_{tail} of the proposed structure is shown in Fig. 25.8.2. $\Gamma_{tail,eff}$ of the proposed structure is compared with a conventional one in Fig. 25.8.3. As shown, by manipulating ISF and NMF, the RMS value of $\Gamma_{tail,eff}$ is significantly reduced which results in much smaller contribution of tail noise to the PN.

In this structure we expect a great improvement of the PN at all offset frequencies. But there are three mechanisms that specifically improve the PN at close-in offset frequencies: (i) Based on ISF theory [4], the n^{th} Fourier series coefficient of ISF (c_n) represents how much noise around the nth-harmonic of oscillation contributes to the PN. So c_0 represents the contribution of flicker noise to the PN. Based on Fourier series coefficients of $\Gamma_{tail,eff}$ in Fig. 25.8.3, c_0 is much smaller in the proposed structure. The reason is that there is a low impedance path to the ground even at very low frequencies, which directly diverts the flicker noise to the ground. (ii) Switching transistors on and off greatly helps with flicker noise suppression [5]. Basically the trap mechanisms that cause flicker noise in CMOS are greatly suppressed by switching the device on and off. (iii) The PMOS transistors at the tail have lower flicker noise.

The contribution of the main transistor noise to the PN is also reduced. Considering the main transistor ISF (Γ_{M1}) in Fig. 25.8.4, Γ_{M1} of the proposed structure is much smaller than that of the conventional one. In the conventional structure, during current transitions the impedance at the common node of the main transistors is very small (almost ground) so noise of M_1 directly injects to the tank and its ISF is large. However, in the proposed structure the impedance at the source of M_1 is larger during transition times so we expect smaller Γ_{M1} during transitions. On the other hand, in the conventional topology when the tail current is completely switched to one side, the corresponding main transistor is source degenerated and its noise circulates in the transistor and does not inject to the tank. So, Γ_{M1} is very small when M_1 is completely on. In the proposed structure the degeneration is still high enough during this time, which makes the noise injection of M_1 negligible. As shown, simulation of Γ_{M1} for both structures also verifies this claim.

A prototype of the proposed structure was fabricated in a 0.13µm CMOS process with a center frequency of 2.4GHz. The inductor size is 2.1nH with a quality factor of 13. One pair of 200fF MOS varactors is used for fine frequency tuning. The VCO consumes 4.2mW from a 1.4V power supply. A reference conventional cross-coupled VCO with the same center frequency and power consumption has been implemented with constraint of best PN performance. Die sizes of both VCOs are the same and each one is 0.27mm×0.34mm. The proposed structure is biased in Class-A, so there is no startup issue and the startup time can be much faster than Class-C oscillators. The bias network is designed to be independent of power supply and process variations as shown in Fig. 25.8.2.

PN is measured using an R&S FSU26 spectrum analyzer. A representative PN measurement for the proposed and conventional structures is shown in Fig. 25.8.5. PN measurement beyond 2MHz is limited by the noise floor of the buffer and measurement equipment. According to measurement results an improvement of 8.2dB at 1MHz and 17dB at 10kHz offset frequencies is achieved. The proposed structure shows a decent FOM of -189.8dBc/Hz at 1MHz and a state-of-the-art FOM of -190.1dBc/Hz at 10kHz offset frequency. The PN variation of the proposed and conventional VCOs vs. tuning voltage is shown in Fig. 25.8.6. As measurements show, PN variation at close-in offset frequencies is much smaller in the proposed structure. A performance comparison of measurement results with state-of-the-art CMOS VCOs is given in Fig. 25.8.6. A micrograph of the fabricated VCOs is shown in Fig. 25.8.7.

Acknowledgement:
We acknowledge the Army Research Lab for their support and STMicroelectronics for silicon donation.

References:

[1] D. Huang, et al, "A frequency synthesizer with optimally coupled QVCO and harmonic-rejection SSBmixer for multi-standard wireless receiver," *IEEE J. Solid-state Circuits*, vol. 46, no. 6, pp. 1307-1320, June 2011.
[2] E. Hegazi, et al, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921-1930, Dec. 2001.
[3] L. Fanori, P. Andreani. "A 2.5-to-3.3 GHz CMOS Class-D VCO," *ISSCC Dig. Tech. Papers*, pp. 346-347. IEEE, Feb. 2013.
[4] T. Lee, A. Hajimiri, "Oscillator Phase Noise: A Tutorial," *IEEE J. Solid-state Circuits*, vol. 35, no. 3, pp. 326-336, Mar. 2000.
[5] E. Klumperink, et al, "Reducing MOSFET 1/f noise and power consumption by switched biasing," *IEEE J. Solid-State Circuits*, vol. 35, no.7, pp. 994-1001, July 2000.

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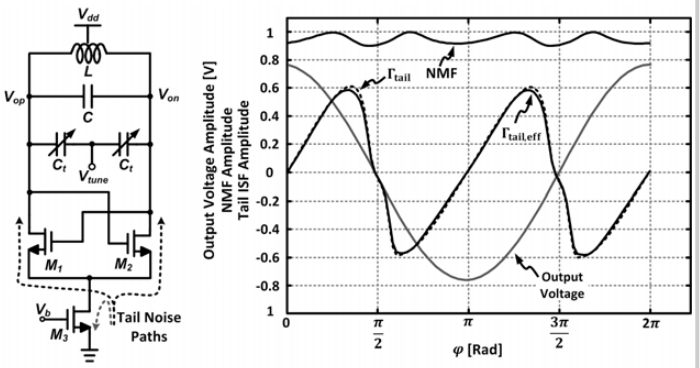


Figure 25.8.1: A conventional cross-coupled oscillator and the tail noise paths (left); Output voltage, ISF, NMF, and effective ISF of the tail transistor (right).

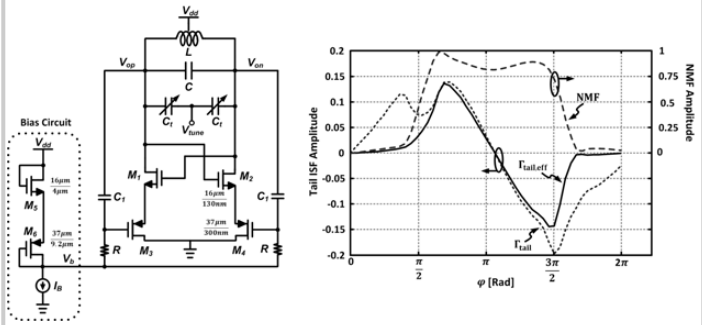
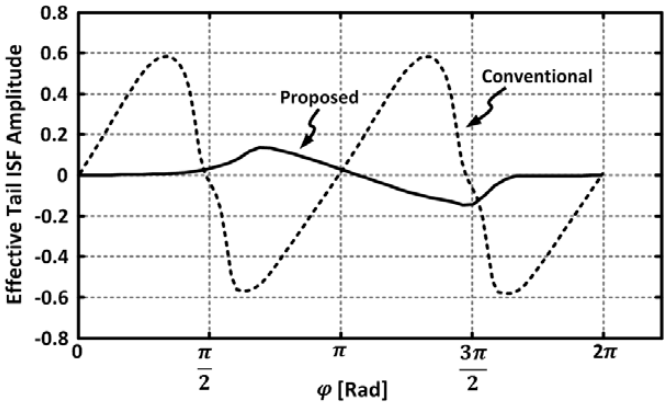


Figure 25.8.2: The proposed structure and the biasing circuit (left); ISF, NMF, and effective ISF of the tail transistors (M3 and M4), (right).



Fourier Series Coef.	C0	C1	C2	C3	C4	C5	C6	RMS
Conventional	0.0060	0.0101	0.5240	0.0016	0.1522	0.0017	0.0355	0.3904
Proposed	0.0002	0.0758	0.0563	0.0027	0.0189	0.0045	0.0087	0.0685

Figure 25.8.3: Effective ISF waveform comparison of the tail transistors in the proposed and conventional structures (top); Fourier series coefficients of the corresponding tail effective ISFs (bottom).

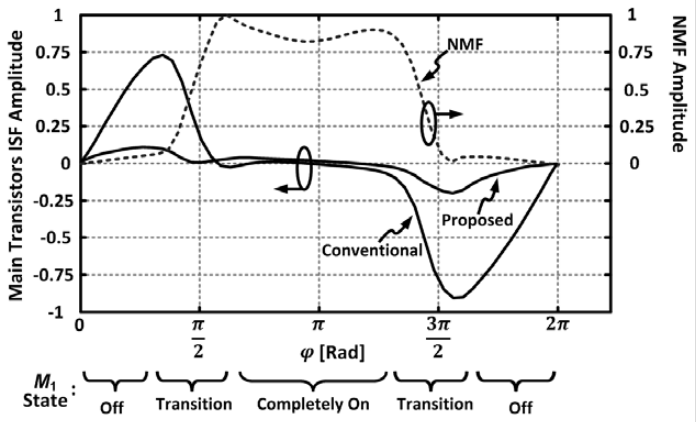


Figure 25.8.4: Main transistor ISF and normalized main transistor current (NMF) of the proposed and conventional structures.

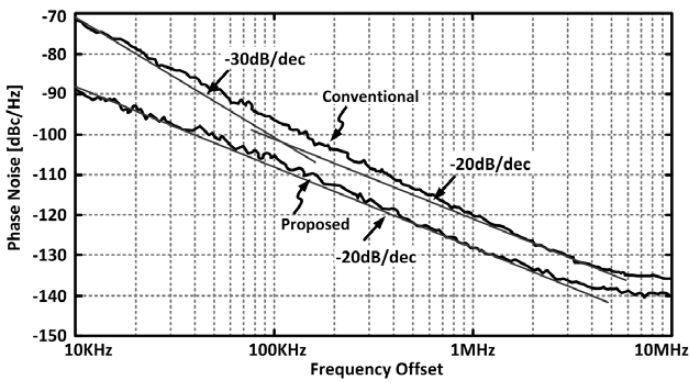
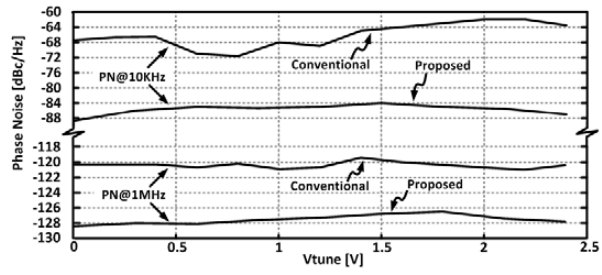


Figure 25.8.5: A phase-noise measurement of the proposed and conventional cross-coupled oscillators.



Publication		Technology	Power [mW]	Frequency [GHz]	PN@10KHz [dBc/Hz]	PN@1MHz [dBc/Hz]	FOM @10KHz [dBc/Hz]	FOM @1MHz [dBc/Hz]	TR [%] *	Core Area [mm^2]
This Work	Proposed	130nm	4.2	2.4	-88.7	-128.4	190.1	189.8	1.7	0.09
	Conventional	130nm	4.2	2.55	-71.6	-120.2	173.5	182.1	1.1	0.09
ISSCC 14		40nm	20	3.72	-77.1	-129.4	175.5	187.7	N/A	0.432
ISSCC 12		55nm	27	3.35	N/A	-132.8	N/A	189.0	N/A	0.49
TCAS—I 12		130nm	4.2	5.6	-68	-122	176.8	190.8	4	0.24
JSSC 11		130nm	1.92	4.9	-73	-123	184.0	194.0	2.5	0.96
JSSC 05		180nm	4.6	2.4	-85	-134	186.0	195.0	1.6	0.36

* Fine tuning range via varactors.

Figure 25.8.6: Phase-noise variation of the proposed and conventional structures vs. tuning voltage (top); Performance comparison of the proposed structure with state-of-the-art CMOS VCOs (bottom).

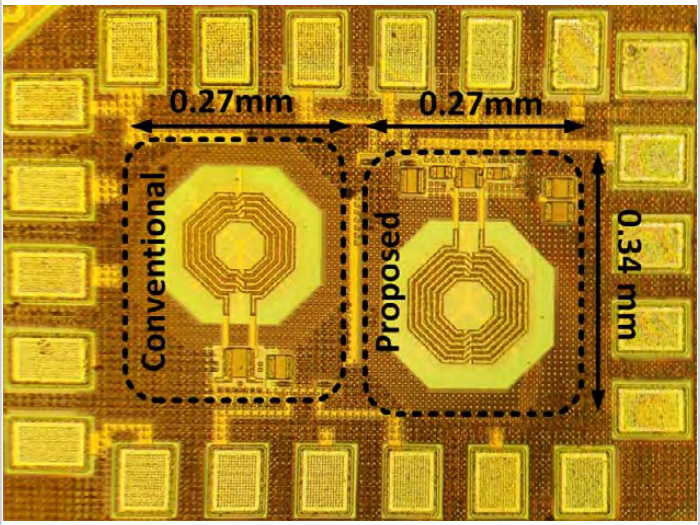


Figure 25.8.7: The die micrograph of the fabricated oscillators.

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