25.6 A 70.5-to-85.5GHz 65nm Phase-Locked Loop with Passive Scaling of Loop Filter

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To support 16-QAM modulation in E-band applications, phase-locked loops (PLLs) are required to have wide a frequency tuning range from 71 to 86GHz and low phase noise of -90dBc/Hz @1MHz [1], which are still very challenging even with aggressive CMOS scaling [2]. Another issue associated with PLLs is the difficulty to integrate on-chip loop filters. Active loop filters are employed to scale down the loop filter capacitors and enable them to be fully integrated on-chip [3]. However, this method suffers from large active noise induced by the op-amp. Moreover, as the capacitance is reduced, the resistor value has to be increased to maintain the same zero frequency, leading to higher thermal noise and limiting achievable scaling factor. Another method is to integrate digital loop filters in all-digital PLLs (ADPLLs) [4]. Unfortunately, the quantization noise of digitally-controlled oscillators (DCOs) becomes a bottleneck to achieve good phase noise due to their limited frequency resolution. Furthermore, E-band DCO oscillation frequency is more sensitive to capacitor variation, making it even more difficult to achieve high frequency resolution. To address these issues, this paper proposes a 70.5-to-85.5GHz PLL with an injection-locked frequency tripler (ILFM3) and passive scaling to increase the effective capacitor for the loop filter by 100 times.

Figure 25.6.1 shows a block diagram of the proposed E-band integer-N PLL with a fully integrated loop filter. A fundamental 26GHz VCO is followed by a balanced differential-input quadrature-output ILFM3 to generate quadrature output signals from 71.5GHz to 85.5GHz. With this topology, the fundamental VCO does not need to provide quadrature outputs and can save half of its power as compared to a QVCO. A divide-by-4 CML divider is inserted between VCO and programmable divider to divide down the frequency. With the ILFM3 and divide-by-4 CML divider, the minimum step of frequency multiplication ratio is 12. Employing a 41.67MHz reference and a programmable divider with division ratio from 143 to 171, the PLL achieves 0.5GHz frequency resolution and is reconfigurable for both 5GHz and 1GHz channels from 71 to 86GHz. The fundamental VCO frequency is controlled and stabilized by a PLL with a passive-scaling dual-path loop filter with a DC control circuit for saturation prevention.

In PLLs, the most difficult part to be integrated on-chip is the integration capacitor, which needs to be extremely large to filter out charge-pump noise and reference spur with sufficient margins. Since a larger capacitor would introduce a smaller voltage with a fixed current flowing through it, a large effective capacitor can be realized with passive scaling using a capacitive voltage divider as depicted in Fig. 25.6.2. The capacitors C_b and C_2 form a voltage divider to divide down the voltage across C_1 and increase the effective integration capacitor from $(C_1+ C_2+ C_b)$ to $C_1 (C_b + C_2)/ C_b \sim C_1 C_2/ C_b$ for the case $C_b \ll C_2$ and $C_b \ll C_1$, which corresponds to a scaling factor of $C_1 C_2/(C_b (C_1+ C_2))$. In this design, C_1=C_2=50pF, and C_b=0.25pF, which results in a scaling factor of 100 and an effective capacitor of 10nF with only 100pF capacitors.

In addition, a dual-path loop filter topology is adopted not only to further reduce the capacitors but also to enable integration capacitor scaling without affecting the zero frequency and the phase margin. Two parallel varactors are incorporated into VCO to combine the dual paths. Figure 25.6.1 shows the PLL open-loop transfer function and the combined dual-path loop filter transfer function. Unlike active loop filters whose noise contribution from active devices increases with the scaling factor [3], the proposed passive scaling technique has lower noise and achieves larger scaling factor.

For the proposed passive scaling, since C_b blocks the DC current, if there is any leakage current flowing through node V_{VCO1}, the output voltage V_{CP} of the charge pump would keep increasing or decreasing and finally become saturated, making the PLL unstable. To solve the problem, a DC control circuit is implemented as shown in Fig. 25.6.2, which consists of two comparators to detect the charge pump output voltage V_{CP}, two D flip-flops with the PLL reference as the clock to load the comparator outputs, and two current sources I_{CP} and I_{VCO1} to set V_{CP}. The working mechanism of the DC control circuit is shown in Fig. 25.6.2. When $V_{CP} < V_L$, the DC control current source I_{CP} is turned on to charge C_1 during time duration t_d, and V_{CP} is increased to V_1 to prevent the charge pump from being saturated. Another current source I_{VCO1} is added to compensate the charging current to keep the control voltage V_{VCO1} unchanged. After t_d, the DC control circuit is turned off, and V_{CP} and V_{VCO1} remain constant. When $V_L<V_{CP}<V_H$, the DC control circuit is turned off for normal operation and does not affect the PLL output phase noise. Finally, for $V_{CP}>V_H$, I_{CP} is turned on to discharge C_1 during time duration t_d, and V_{CP} is decreased to V_3. At the same time, I_{VCO1} is enabled to compensate the discharging current to maintain the same control voltage V_{VCO1}. After t_d, the DC control circuit is turned off, and V_{CP} and V_{VCO1} stay constant. Since the control voltage V_{VCO1} is kept constant for all values of V_{CP}, the PLL transfer function would not be affected by the DC control circuit. For the DC control circuit to work well, it is necessary that the ratio of the two currents I_{CP} and I_{VCO1} is designed to be the same as the scaling factor, which is limited due to the matching requirement and thus limits the maximum achievable scaling factor for the loop filter's capacitor.

Figure 25.6.3 shows the proposed mixer-based balanced differential-in quadrature-out injection-locked frequency tripler (ILFM3). A push-push injection-locked frequency doubler (ILFM2) with balun is implemented to generate differential outputs at double frequency, which are divided down by injection-locked frequency dividers (ILFDs) to obtain quadrature signals. The triple frequency is generated by mixing the ILFD output with the ILFM2 output and fed into injection-locked oscillators (ILOs). Because of process variation and inaccurate modeling, the locking range of ILFM3 has to be wide enough to cover the desired frequencies with sufficient margins. Compared to the conventional solution with a hard limiter whose maximum 3rd-harmonic generation efficiency is only $4/(3\pi)$ (~42%), the mixer-based scheme can achieve efficiency of $8/\pi^2$ (~81%) and thus larger locking range. Moreover, the hard limiter not only needs quadrature input but also has an output IQ mismatch at $3f_o$ being triple that of the input I/Q mismatch at f_o. In contrast, the proposed technique avoids a need for a quadrature VCO and enables the output IQ mismatches at $3f_o$ to be almost the same with the IQ mismatches at the ILFD output at f_o. Unlike the injection-locked frequency tripler in [1], which only provides differential injection to a quadrature oscillator, this scheme has small frequency-independent phase error because the injection to the frequency tripler ILFM3 is symmetrical for both I and Q paths. As shown in Fig. 25.6.3, the switched transformer is employed in the ILFM2 and ILO to further extend the locking range by creating multiple frequency bands.

The PLL was fabricated in a CMOS 65nm GP process and consumes 54.5mW. The fundamental PLL consumes 31.2mW at 1.2V (24mW for VCO, 2.4mW for CML, 0.5mW for programmable divider, and 4.2mW for charge pump and DC control circuit) while the ILFM3 consumes 23.3mW at 1V. The fundamental PLL frequency tuning range is measured from 23.5GHz to 30.5GHz. The ILFM3 locking range is measured from 59.25GHz to 85.5GHz with 0dBm input power. With a frequency tuning step of 0.5GHz, the PLL covers the whole frequency range from 71 to 86GHz for ten 1GHz channels and two 5GHz channels. As shown in Fig. 25.6.4, the PLL output phase noise at 1MHz offset is measured to be -94.6dBc/Hz at 73.5GHz. Figure 25.6.5 shows the measured PLL frequency spectrum with a 50KHz effective loop bandwidth. The sideband rejection ratio contributed by the IQ amplitude and phase errors is -35dBc, and the fundamental PLL reference spur is around -45dBc. Figure 25.6.6 summarizes and compares the performance with existing state-of-the-art PLLs. The proposed passive scaling technique increases the effective capacitor in the loop filter by 100 times while the active scaling technique only achieves 4 times scaling. Moreover, thanks to the proposed ILFM3, the proposed PLL has wider frequency tuning range than [2] and can satisfy the frequency tuning range requirement for 71-to-86GHz E-band applications. Figure 25.6.7 shows the PLL die micrograph. The PLL occupies 0.6mm^2 core chip area with only 0.12mm^2 for the loop filter even with 50kHz loop bandwidth and 10nF effective integrator capacitor.

Acknowledgments:
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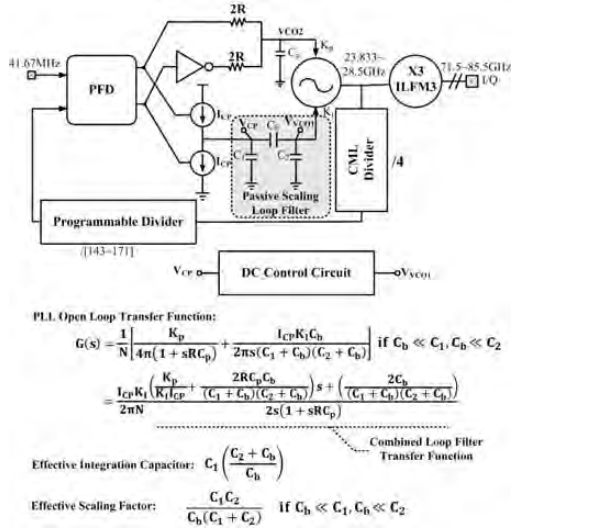

Figure 25.6.1: Block diagram of the proposed E-band PLL with a dual-path loop filter and capacitor passive scaling.

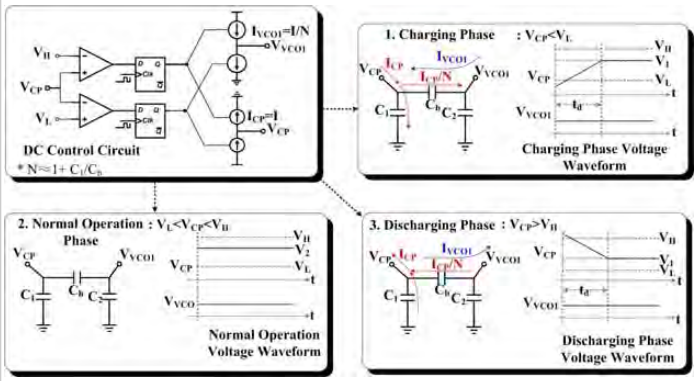

Figure 25.6.2: Block diagram and working mechanism of the proposed DC control circuit for the passive-scaling dual-path loop filter

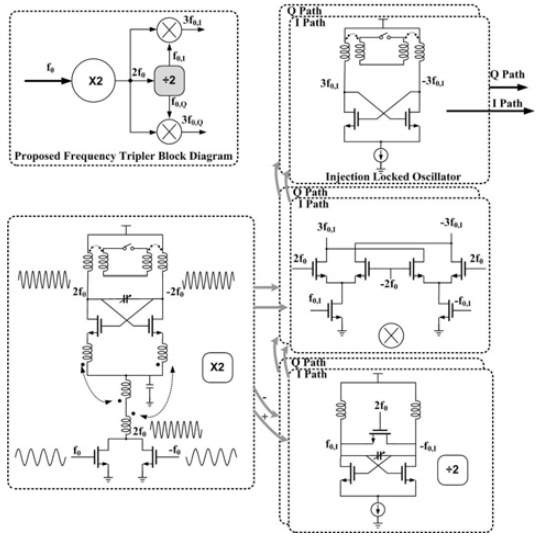

Figure 25.6.3: The implementation of the proposed balanced differential-input quadrature-output frequency-tripler ILFM3.

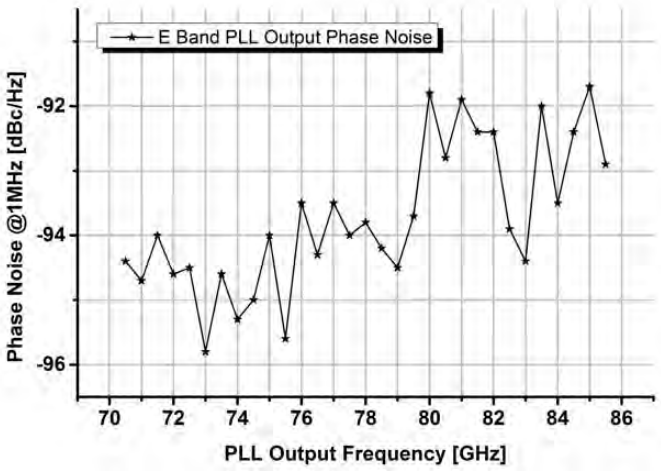

Figure 25.6.4: Measured output phase noise at 1MHz offset vs frequency.

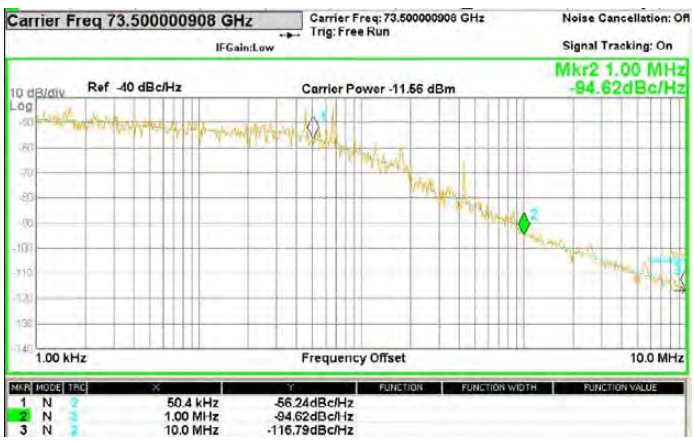

Figure 25.6.5: Measured PLL output spectrum at 73.5GHz.

	[2] JSSC '08, Lee	[3] CICC '13, Catli	[4] ISSCC '13 , Wu	ISSCC '14, Szortyka	This Work
Freq. [GHz]	73.4-73.7	8-12.2	56.4-63.4	53.8-63.3	70.5 – 85.5
Ref. Freq. [MHz]	1146-1151	156.25	100	40	41.67
TR [GHz,%]	0.3, 0.4%	4.2, 41.6%	7, 11.6%	9.5, 16%	15, 19.2%
BW [MHz]	2-3	1.3-6.5	0.1	1	0.05
PN @1MHz [dBc/Hz]	-92	-114	-90	-88.3	-91.7 ~ -95.8
VDD [V]	1.45	1	1.2	0.9	1.2/1
Power [mW]	88	15.5/16.5	48	42	54.5
Loop Filter Scaling Factor	N/A	4 (Active loop filter)	Digital PLL	N/A	100
FOM_T *	-142	-200	-170	-172	-182
Output Type	Differential	Differential	Differential	Quadrature	Quadrature
Core Area [mm²]	0.8	0.093	0.48	0.16	0.6
Process	90nm CMOS	28nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS

$*FOM_T = PN - 20\log\left(\frac{f_0}{\Delta f} \times \frac{FTR}{10\%}\right) + 10\log\left(\frac{Power}{1mW}\right)$

Figure 25.6.6: Measurement summary and comparison with existing state-of-the-art PLLs.

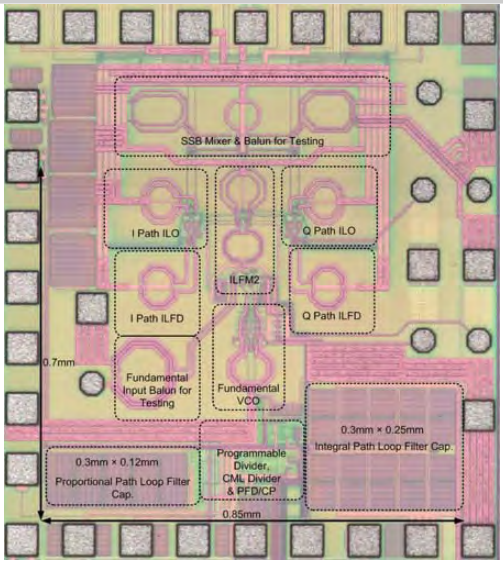

Figure 25.6.7: Die micrograph.

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