

25.2 A 2.2GHz -242dB-FOM 4.2mW ADC-PLL Using Digital Sub-Sampling Architecture

Teerachot Siriburanon, Satoshi Kondo, Kento Kimura, Tomohiro Ueno, Satoshi Kawashima, Tohru Kaneko, Wei Deng, Masaya Miyahara, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Tokyo, Japan

This paper presents an all-digital phase-locked loop (PLL) using a voltage-domain digitization realized by an analog-to-digital converter (ADC). It consists of an 18b Class-C digitally-controlled oscillator (DCO), 4b comparator, digital loop filter (DLF), and frequency-locked loop (FLL). Implemented in 65nm CMOS technology, the proposed PLL reaches an in-band phase noise of -112dBc/Hz and an RMS jitter of 380fs at 2.2GHz oscillation frequency. An FOM of -242dB has been achieved with a power consumption of only 4.2 mW.

Figure 25.2.1 shows a conceptual diagram of the proposed ADC-based all-digital PLL (ADC-PLL), which is based on a voltage-domain digitization rather than a time-domain counterpart. TDCs or PFD/CPs in conventional PLLs are replaced by an ADC, which has advantages in terms of a finer resolution and lower power consumption. The bang-bang PLL (BB-PLL) [1] is one of the simplest architectures for digital PLLs but it suffers from the degradation of in-band phase noise. The TDC-based all-digital PLL (TDC-PLL), based on the time-domain digitization, has been widely explored [2]-[6]. However, the jitter performance, *i.e.*, in-band phase noise, of recently-published TDC-PLLs still suffers from the limited TDC resolution. This paper demonstrates that the voltage-domain digitization used in the proposed ADC-PLL is more feasible for a digital PLL, at least, in the present CMOS technology to achieve lower in-band phase noise while consuming low power.

Figure 25.2.2 shows an ADC-based phase detector (ADC-PD), which consists of an isolation buffer, sample-and-hold circuits, a pre-amplifier, and a 4b flash ADC. Only the isolation buffer works at the oscillation frequency of the DCO while the other blocks operate at the reference clock. Comparing to the time-domain digitization, the voltage-domain operation is advantageous due to capabilities of (1) sample-and-hold, (2) amplification, and (3) sub-ranging. This helps the phase detection to achieve finer resolution and wider dynamic range with low power consumption. Since the voltage-domain signal can be easily sampled-and-held, the proposed digital conversion has only to operate at a reference frequency as it is operating in sub-sampling operation. To obtain a finer resolution, the hold signal can be easily amplified by a linear operational amplifier unlike a linear time amplification which is not easily realized. In addition, the digital conversion can be parallelized and sliced in the voltage-domain. This gives an advantage to achieve a shorter delay and a finer resolution. In this implementation, the 4b flash ADC with resistive averaging has a 10mV minimum resolution, and each dynamic comparator achieves a 2.5mV_{rms} offset without any offset calibration according to the transient-noise simulation [7]. The voltage resolution can be magnified by the preamplifier to further improve the equivalent time resolution (Δt), which can be calculated by the following equation:

$$\Delta t \cong \frac{1}{G} \cdot \frac{V_{\text{range}}}{2^N \cdot V_{\text{DCO}}} \cdot \frac{1}{2\pi f_{\text{DCO}}}$$

where V_{range} is the full input reference voltage range of an ADC, V_{DCO} is the oscillation amplitude, N is the number of bits of the ADC, f_{DCO} is the oscillation frequency, and G is the gain of a preamplifier. In the case of 2.2GHz oscillation, the equivalent time resolution can be as fine as 0.23ps assuming oscillation amplitude of 1V, preamplifier gain of 20 and ADC resolution of 50mV. In addition, a re-conversion can be applied with a smaller gain in case of over-range. This means that a very fine time resolution with a wide range can be achieved by using an ordinary ADC.

Figure 25.2.3 shows the circuit schematic of an 18b push-pull Class-C DCO [8], where 8 bits are assigned for the frequency-locked loop (FLL) as the coarse tuning, 7 bits are assigned for the medium tuning, and 3 bits are used for the fine tuning with a delta-sigma modulation (MASH 1-1-1). To achieve a low power while maintaining low phase noise, an LC push-pull Class-C topology is employed even though a ring-type DCO can also be used in the proposed ADC-PLL. The push-pull Class-C VCO has an issue of the amplitude imbalance [8,9], so a replica-bias circuit is proposed for the amplitude balancing as well as the start-up compensation. At the oscillation start-up of conventional push-pull class-C VCOs [8], the voltage amplitude is small, and the gate biases could stay lower than the threshold voltage due to the Class-C biasing. By using the replica-bias circuit, the gate bias voltages for PMOS and NMOS cross-coupled pairs are both enhanced at the oscillation start-up and adaptively changed as it enters the Class-C operation. The voltage imbalance caused by g_m mismatch is also improved by the proposed replica biasing scheme.

Figure 25.2.4 shows the entire block diagram of the proposed ADC-PLL. It is composed of an FLL for frequency acquisition [10] and the core phase-locking loop using an ADC-PD, which can be understood as a digital version of a sub-sampling PLL. The ADC-PD samples and digitizes the oscillation signal at every rising edge of the reference clock so that the crossing point of differential oscillation signals meets the reference clock edge as shown in Fig. 25.2.2. The sub-sampling loop can lock at every integer multiple of the reference clock. In addition, a dead zone in the FLL loop filter (LF) has been implemented so as not to disturb the phase locking of the core ADC-PD loop. The DCO has an 8b capacitor bank for the FLL coarse tuning which is controlled by the 12b frequency control word. The frequency resolution of FLL bits is designed to be less than the reference frequency, which is 10MHz for 40MHz reference. The 12b counter is used for the frequency detection. In the phase-locked loop, the loop filter in the phase-locking path generates a 7b acquisition code and a 6b tracking code. The tracking code controls 3 delta-sigma modulated bits for fine-tuning the DCO. In the proposed architecture, only a DCO and an ADC-PD require analog design while other building blocks are digital circuits that have been synthesized with a standard cell library.

Figure 25.2.5 shows the measured phase noise plots and the frequency spectrum at 2.2GHz evaluated by a signal source analyzer (Agilent E5052B), and a spectrum analyzer (Agilent E4407B), respectively. The measured in-band phase noise is -112dBc/Hz at 300kHz offset, and the integrated jitter (10 kHz to 40 MHz) is 0.38ps. The frequency tuning range of the DCO is 2.15 to 2.35 GHz. The reference clock is 100MHz, and the reference spur is -74dBc. The power consumption of the DCO is 1.5mW from a 1.0V supply. The isolation buffer and preamplifier consume 0.5mW, and the 4b flash ADC consumes 1.2mW. The digital blocks consumes 1.0mW, including the digital loop filters, frequency counter, and delta-sigma modulator.

Figure 25.3.6 shows a comparison table for the state-of-the-art TDC-based digital PLLs. The proposed ADC-PLL achieves the lowest in-band phase noise performance while consuming only 4.2mW. The figure of merit (FOM) is -242dB at 2.2GHz output frequency, where the FOM is defined as $10\log[(\sigma_j/1s)^2 \cdot (P_{\text{DC}}/1mW)]$, σ_j is the integrated jitter, and P_{DC} is the DC power consumption. Figure 25.2.7 shows the die micrograph. The ADC-PLL is fabricated in 65nm CMOS technology. The areas for DCO, ADC-PD, and digital blocks are 0.13mm², 0.01mm², and 0.01mm², respectively.

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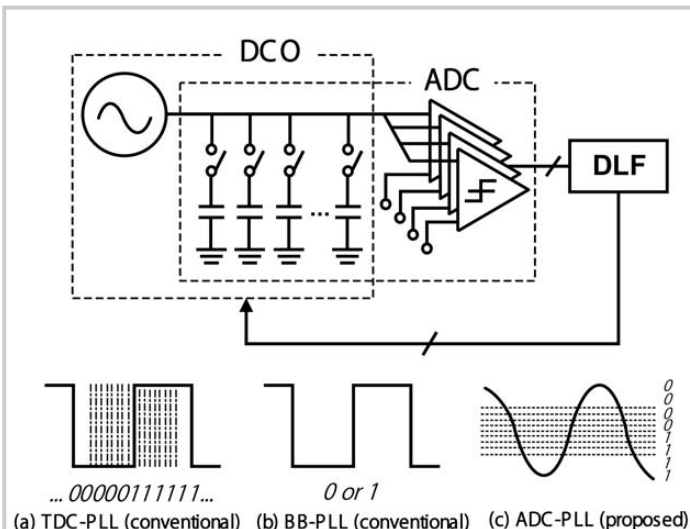


Figure 25.2.1: Conceptual diagram of proposed ADC-PLL.

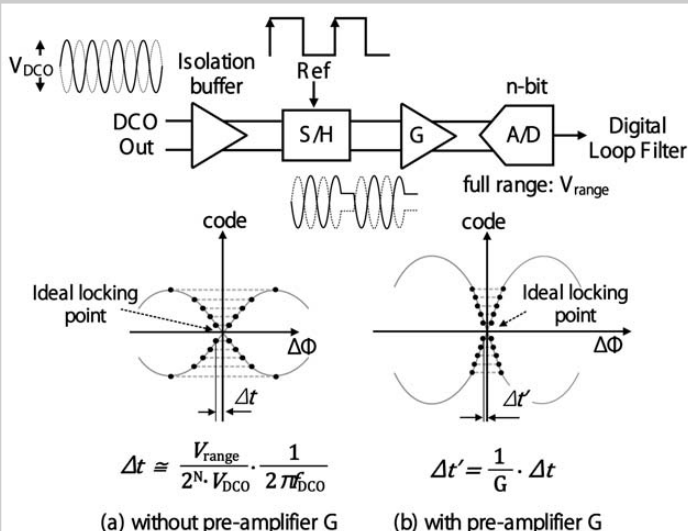


Figure 25.2.2: Phase detector using analog-to-digital converter (ADC-PD).

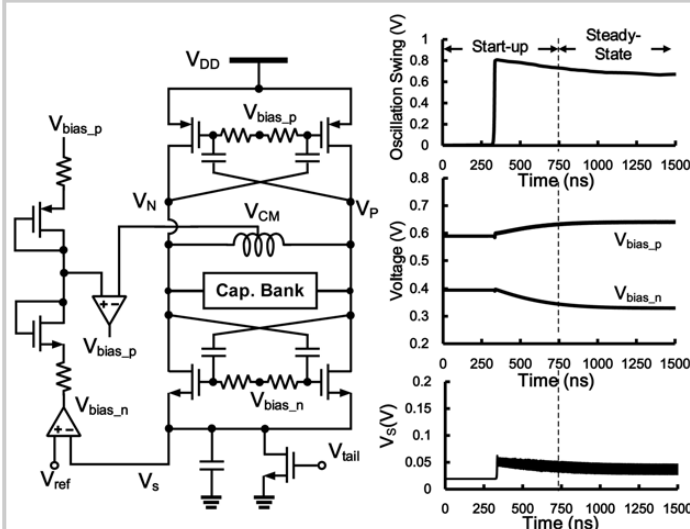


Figure 25.2.3: Schematic of Class-C push-pull DCO with its relevant waveforms.

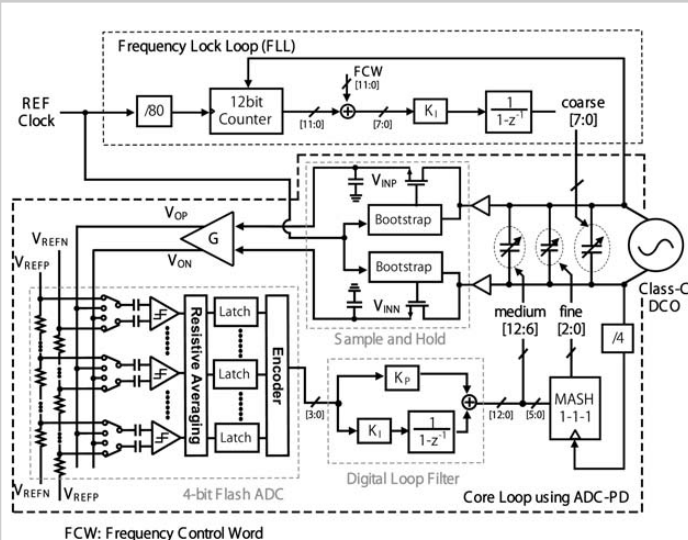


Figure 25.2.4: Block diagram of the proposed ADC-PLL.

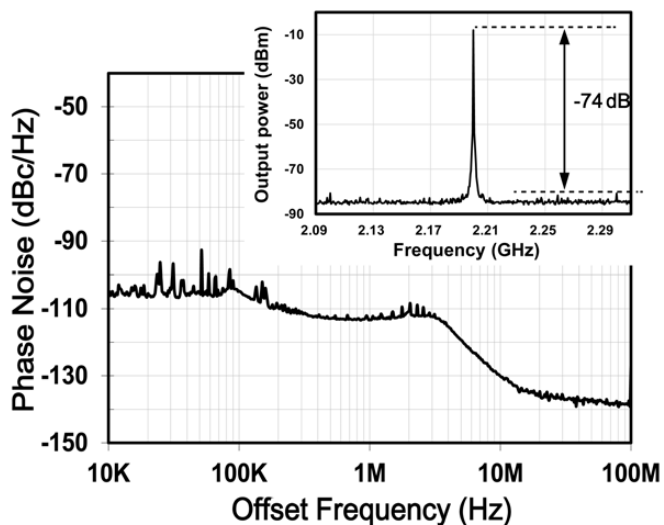


Figure 25.2.5: Measured phase noise and frequency spectrum at 2.2GHz.

	This Work	JSSC'09 [2]	ISSCC'11 [3]	JSSC'13 [4]	ISSCC'14 [5]	ISSCC'14 [6]
Topology	ADC-based	TDC-based	TDC-based	TDC-based	TDC-based	TDC-based
Type	Integer	Fractional	Integer	Fractional	Fractional	Fractional
Freq.	2.2GHz	3.6GHz	5.3GHz	2.7GHz	2.4GHz	5.8GHz
RMS Jitter	380fs	200fs	220fs	230fs	1.71ps	175fs
In-band Phase Noise	-112 dBc/Hz	-107 dBc/Hz	-101 dBc/Hz	-110 dBc/Hz	-90 dBc/Hz	-105 dBc/Hz
Ref. Spur	-74dBc	-65dBc	-67dBc	-75dBc	-70dBc	N/A
PLL FoM	-242dB	-237dB	-239dB	-240dB	-236dB	-244dB
Power Dissipation	4.2mW	47mW	24mW	17mW	0.9mW	12.9mW
Area	0.15mm ²	0.95mm ²	0.91mm ²	0.62mm ²	0.20mm ²	N/A

Figure 25.2.6: Performance comparison with the state-of-the-art digital PLLs.

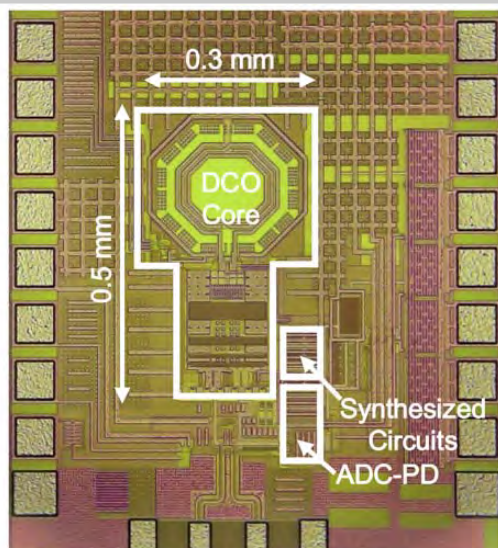


Figure 25.2.7: Die micrograph.