24.4 A 6.5Gb/s Shared Bus Using Electromagnetic Connectors for Downsizing and Lightening Satellite Processor System by 60%

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Processor systems that are mounted in satellites must be small and light, having high data transfer rates, and high storage capacity [1]. A small reduction in size and weight could reduce the cost of launching a satellite by a significant amount. The next generation of earth observation satellites will require data transmission rates to a maximum of 20Gb/s and at least one terabyte of storage capacity. The volume, weight, and communication speed of the processor system is determined by the backplane connectors (Fig. 20.4.1). It is difficult to achieve a connector that can pass signals of 2.5Gb/s or more. The signal reflection that occurs when signals are branched at connectors and at the wire stubs of branches decreases the transmission speed, so only point-to-point connections are possible. Once the satellite is launched, repair or replacement is not possible, and system redundancy is introduced. Accordingly, 512 backplane wires would be required. The signal connector would require 1,024pins, including the ground pins used to prevent crosstalk, and would be 512mm wide, which is even wider than the circuit board of each module.

We have developed two types of electromagnetic connectors; a bidirectional transmission line couplers (BD-TLC) for a shared bus backplane (Fig. 24.4.1), and a single-ended to differential conversion TLC (SDC-TLC) for a memory module (Fig. 24.4.2). The BD-TLC provides a noncontact data connection. It has a simple structure that is robust against shock, and it is also small and light. Impedance matching enables bi-directional signal branching and a shared bus can be employed to reduce the number of wires. With a proposed transceiver described later, a data rate of 6.5Gb/s is possible and the number of wires can be reduced from 512 to 32 (a factor of 1/16). The TLC's can be arranged at a pitch of 2.8mm, enabling a connector width of 47.6mm. Volume of the TLC connectors (47.6mm x 7mm x 0.4mm) is reduced by a factor of 1/246 compared to the conventional connectors (512mm x 8mm x 8mm). Because that dimension is smaller than the memory module, the width of the backplane substrate can be made to the size of the memory module. As described later, the memory modules can also be made smaller so that the width of the processor system can be reduced by 60% from 610mm to 240mm.

To reduce the width of the memory modules, the single-ended to differential conversion TLC (SDC-TLC) was developed as a high mounting density coupler (Fig. 24.4.2). It can convert a single-ended signal to a differential signal and can be used in a multidrop bus configuration. Five memory devices and a memory controller in the FPGA can be connected by a bus, so the number of signal wires can be reduced by 80% and the width of the memory module can be reduced to 240mm. In a multidrop bus configuration, the incoming DDR4 single-ended signal at each branch is converted to a differential signal by the SDC-TLC, and restored to a digital signal by a differential receiver. There is high margin against the PVT variations and high tolerance to common-mode noise.

Here we explain the SDC-TLC operating principle for the conversion from a single-ended signal to a differential signal (Fig. 24.4.2). The single-ended signal input from port 1 to electrode 1 generates a signal in electrode 3 that has the same symbol but opposite direction. That signal is completely reflected at the shorted end of the electrode, which reverses the phase by 180°, and the signal proceeds to port 3 as an inversion of the input signal. When the input signal proceeds past the midpoint of electrode 1, it generates a signal in electrode 2 that has the same symbol but opposite direction. That signal has the same phase as the input signal and proceeds to port 2. Accordingly, the single-ended signal that was input at port 1 appears as a differential signal at ports 2 and 3. Similarly, in the reverse direction, a differential signal input from port 2 and port 3 arrives at port 1 as a single-ended signal. Because two couplers are arranged in series, the layout area in the length direction is twice as long. However, only one fourth the area is needed in the width direction, so the SDC-TLC occupies only 4.2mm², reduced by 55% compared to the conventional TLC [2].

With the backplane that uses the BD-TLC and the memory modules that use the SDC-TLC, all signals pass through a TLC two times. Because the TLC has a low cut characteristic of 20dB/dec, the signal is subjected to first-order differentiation at each pass through the TLC. In a shared bus, the signal is subjected to second-order differentiation by two passes through the TLCs. That results in double pulses at the receiving end. Because double pulses are in the TLC passband, the maximum communication speed is decreased by half. As the maximum reported data transfer rate of the multidrop bus with TLC is 7Gb/s [2], the expected data rate for two passes through the TLCs is 3.5Gb/s. That makes it difficult to achieve 6.5Gb/s required for the shared bus.

A low-frequency compensation equalizer (LFC-EQ) has been developed to solve this problem (Fig. 24.4.3). An NMOS cross-coupled pair generates negative conductance of $-g_{m.EQ}$. When $-g_{m.EQ}$ is set equal to $1/R_1$, they cancel out, and only C_1 remains as a load of the amplifier. The transfer function thus becomes $g_{m.AMP}/j\omega C_1$ to yield low-frequency compensation characteristics. The DC gain (at ω=0), however, becomes infinity, and input offsets generate saturated outputs of 1 or 0. A high-pass filter that is composed of C_2 and R_2 is applied to reduce the DC gain, which yields the following transfer function; $g_{m.AMP}/(j\omega C_1 + g_{m.EQ}/(1+j\omega C_2R_2))$. The DC gain (at ω=0) is $g_{m.AMP}/g_{m.EQ}$. In frequency ranges where $g_{m.EQ}/(1+j\omega C_2R_2) << j\omega C_1$, the transfer function approximates to $g_{m.AMP}/j\omega C_1$. Simulations indicate 20dB/dec low frequency emphasis is obtained over a wide range of 0.8GHz to 10GHz. The low frequency cutoff characteristic of 40dB/dec through two TLCs is moderated to 20dB/dec, so that ISI is suppressed and wide eye opening is obtained at 6.5Gb/s.

A transceiver chip was fabricated in 65nm CMOS technology (Fig. 24.4.7). Operating under a 1.2V supply, the power consumption was 31.8mW. The BD-TLCs were formed on a FPC and an FR4 substrate. The SDC-TLCs were formed on a FR4 substrate. One-axis vibration tests were performed based on the MIL standard [3] (Fig. 24.4.4). Under the same vibration (20.76Grms) as exists during the launch of a satellite, no change in the TLC characteristics was confirmed. It was also confirmed that no single bit failure occurred during the period of launch (60 seconds) at a data rate of 100Mb/s. The electromagnetic interference from the BD-TLC was also evaluated. A PRBS 2^{31}-1 signal was transmitted at 6.5Gb/s via the BD-TLC. The measurement results confirmed that the radiation was below the thermal noise level (-111dBm) at distances greater than 9mm. It was also confirmed that a GPS signal is not affected at a separation of 5.5mm when -30dB shielding is employed. Communication tests for the backplane performed with 6 modules connected confirmed that the BER was less than 10^{-12} for 6.5Gb/s for all modules (Fig. 24.4.5). The timing margin at the BER of 10^{-12} was 0.31UI. Tests for the memory module were performed at 3.2Gb/s to match the DDR4 memory interface. The BER with 6 modules connected was confirmed to be less than 10^{-12} with a timing margin of 0.67UI. A comparison with the performances reported at the recent ISSCC [2,4-6] (Fig. 24.4.6) shows that the smallest area (0.09mm²/Gbps) and the lowest energy consumption (4.9pJ/b) were achieved.

Acknowledgements:
This work was supported by CREST/JST.

References:
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[2] W. Yun, *et al.*, "A 7Gb/s/Link Non-Contact Memory Module for Multi-Drop Bus System Using Energy-Equipartitioned Coupled Transmission Line," *ISSCC Dig. Tech. Papers*, pp. 52-53, Feb. 2012.
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[5] A. Kosuge, *et al.*, "An Electromagnetic Clip Connector for In-Vehicle LAN to Reduce Wire Harness Weight by 30%," *ISSCC Dig. Tech. Papers*, pp. 496-497, Feb. 2014.
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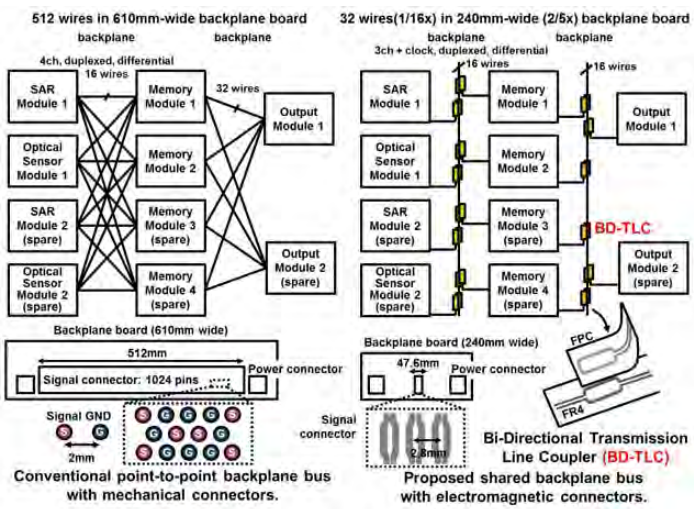

Figure 24.4.1: Non-contact shared backplane bus using differential bi-directional transmission line coupler (BD-TLC).

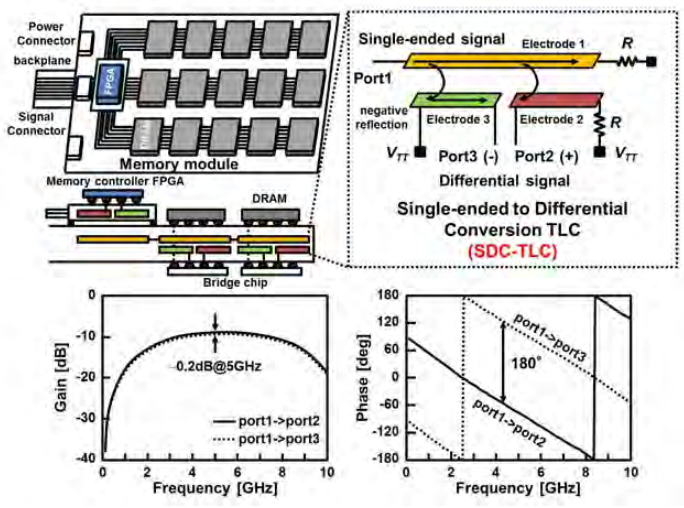

Figure 24.4.2: Memory module using single-ended-to-differential conversion transmission-line coupler (SDC-TLC).

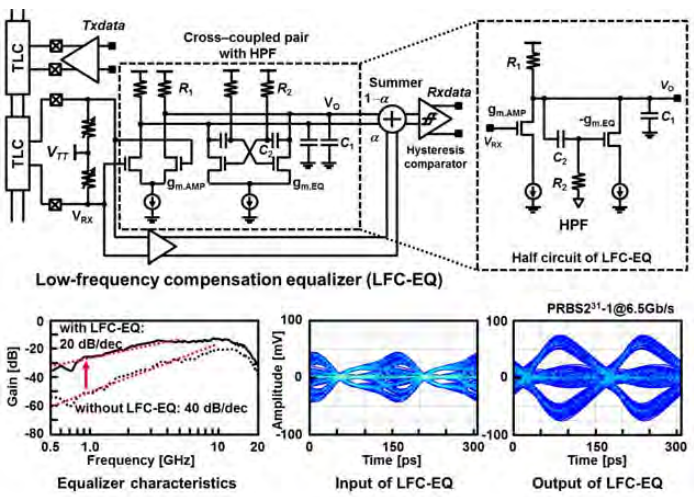

Figure 24.4.3: Transceiver circuits with low-frequency compensation equalizer (LFC-EQ).

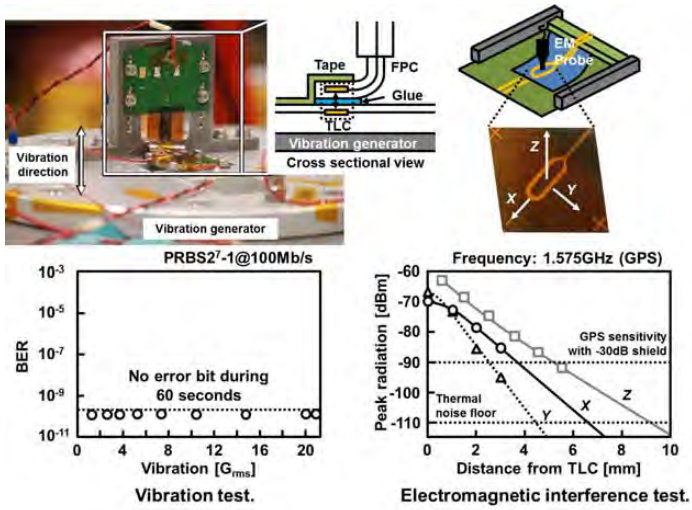

Figure 24.4.4: Measured vibration tolerance and radiation of TLC.

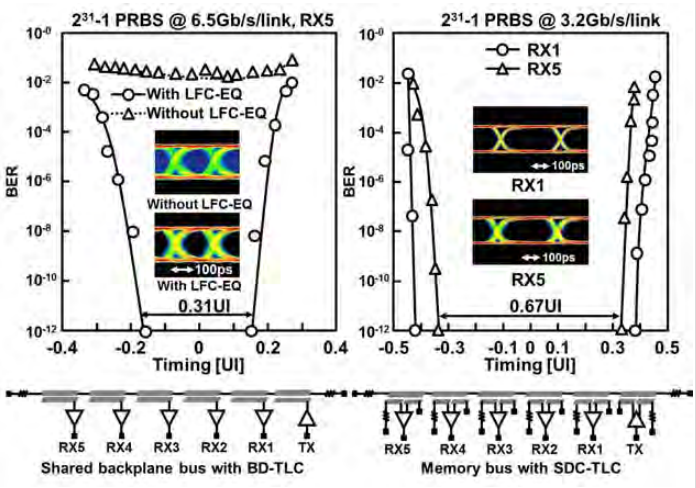

Figure 24.4.5: Measured timing bathtub curves.

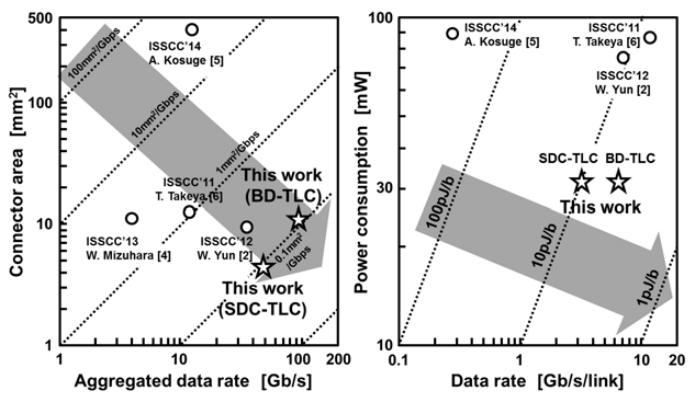

Figure 24.4.6: Performance comparison.

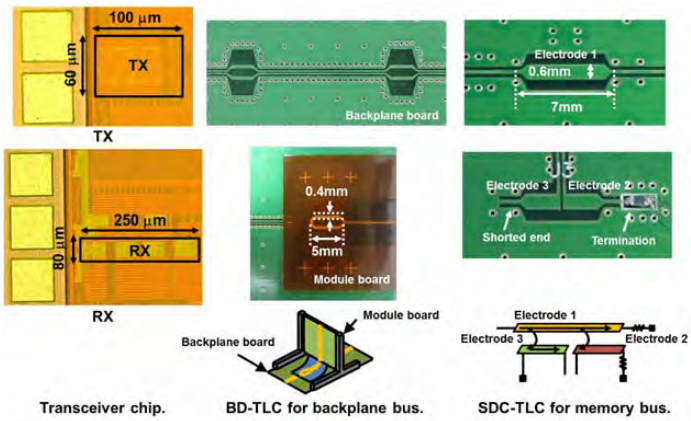

Figure 24.4.7: Photographs of transceiver chip and TLCs.

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Session 25 Overview: *RF Frequency Generation from GHz to THz*

RF SUBCOMMITTEE

Session Chair: *Payam Heydari, University of California, Irvine, CA*

Session Co-Chair: *Taizo Yamawaki, Hitachi, Tokyo, Japan*

Frequency generation circuits are ubiquitous building blocks in communication, sensing, and imaging systems. This session covers the latest advances in frequency generation, targetting reduction of noise, chip area, and power consumption in frequency synthesizers and VCOs. The session includes an E-band phase-locked-based frequency synthesizer that employs passive scaling to increase loop-filter capacitance, a phase-locked-based transmission array at 320GHz frequency, and a highly stable thin-film-based acoustic resonator achieving a stability of ±3 ppm from 0 to 90°C. Two papers describe techniques for reducing the effects of flicker noise in oscillators, another describes quantization noise cancellation in a fractional-N PLL, and another reduces PLL noise by manipulating impulse sensitivity and noise modulating functions of transistors. One paper addresses all-digital PLL design using voltage-mode digitization, and another describes inductorless PLL design to reduce power consumption.

25.1 A Highly-Digital Frequency Synthesizer Using Ring-Oscillator Frequency-to-Digital Conversion and Noise Cancellation **1:30 PM**

C. Weltin-Wu, Analog Devices, San Jose, CA and University of California, San Diego, CA

Paper 25.1 presents a highly-digital 3.5GHz fractional-N PLL with dual-mode ring oscillator frequency-to-digital conversion and quantization noise cancellation. Its phase noise is -93, -126, and -151dBc/Hz at 100kHz, 1MHz, and 20MHz offsets, respectively, its largest in-band spurious tone is -60dBc, and its power dissipation is 15.6mW.

25.2 A 2.2GHz -242dB-FOM 4.2mW ADC-PLL Using Digital Sub-Sampling Architecture **2:00 PM**

T. Siriburanon, Tokyo Institute of Technology, Tokyo, Japan

In Paper 25.2, Tokyo Institute of Technology presents an all-digital PLL that employs a voltage-domain digitization realized using an ADC. The PLL achieves an in-band phase noise of -112dBc/Hz and an rms jitter of 380fsec at 2.2GHz.

25.3 A VCO with Implicit Common-Mode Resonance **2:30 PM**

D. Murphy, Broadcom, Irvine, CA

In Paper 25.3, Broadcom presents an LC VCO that uses a common-mode resonance at twice the oscillation frequency to reduce the impact of flicker noise. A 3GHz prototype VCO exhibits -139.7dBc/Hz at 1MHz offset.

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25.4 A 1/f Noise Upconversion Reduction Technique Applied to Class-D and Class-F Oscillators **2:45 PM**

M. Shahmohammadi, Delft University of Technology, Delft, The Netherlands

In Paper 25.4, Delft University of Technology presents another technique based on setting up a trap for higher harmonics to lower the flicker noise contribution on the oscillator phase noise. The 4GHz VCO prototype achieves -123.4dBc/Hz at 1MHz offset.

25.5 A 320GHz Phase-Locked Transmitter with 3.3mW Radiated Power and 22.5dBm EIRP for Heterodyne THz Imaging Systems **3:15 PM**

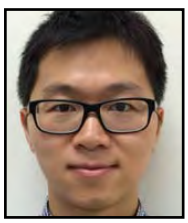
R. Han, Cornell University, Ithaca, NY
and Massachusetts Institute of Technology, Cambridge, MA

In Paper 25.5, Cornell University, MIT and STMicroelectronics present a 320GHz phase-locked-based 16-transmitter array in a 0.13µm SiGe process. The radiator achieves DC-to-RF efficiency of 0.54% and an EIRP of 22.5dBm.

25.6 A 70.5-to-85.5GHz 65nm Phase-Locked Loop with Passive Scaling of Loop Filter **3:45 PM**

Z. Huang, Hong Kong University of Science and Technology, Hong Kong, China

In Paper 25.6, HKUST and Tsinghua University present a CMOS E-band PLL with passive scaling of the loop filter to increase the filter's effective capacitance. The core PLL occupies 0.6mm^2 of chip area with its loop filter taking 0.12mm^2 of this area. It exhibits better than -91.7dBc/Hz of phase noise at 1MHz offset.



25.7 A 2.4GHz 4mW Inductorless RF Synthesizer **4:15 PM**

L. Kong, University of California, Los Angeles, CA

In Paper 25.7, UCLA presents a CMOS inductorless 2.4GHz frequency synthesizer that can achieve locked phase noise of -114dBc/Hz at 1MHz offset with 4mW of power consumption.

25.8 A 2.4GHz VCO with FOM of 190dBc/Hz at 10kHz-to-2MHz Offset Frequencies in 0.13µm CMOS Using an ISF Manipulation Technique **4:30 PM**

A. Mostajeran, Sharif University of Technology, Tehran, Iran
and Cornell University, Ithaca, NY

In Paper 25.8, Sharif University of Technology and Cornell University present a CMOS 2.4GHz VCO that achieves low phase noise by manipulating the ISF and NMF of transistors. The VCO achieves -128.4dBc/Hz phase noise at 1MHz offset.

25.9 A ±3ppm 1.1mW FBAR Frequency Reference with 750MHz Output and 750mV Supply **4:45 PM**

K. A. Sankaragomathi, University of Washington, Seattle, WA

In Paper 25.9, the University of Washington presents a CMOS 750MHz thin-film bulk acoustic resonator (FBAR) that achieves a stability of ±3 ppm from 0 to 90°C. A new temperature sensor is implemented that achieves 1.75mK resolution at 100msec sensing.